

FIG. 1A
(Prior Art)

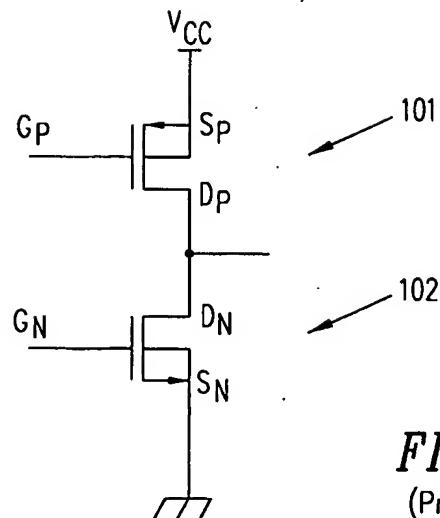


FIG. 1B
(Prior Art)

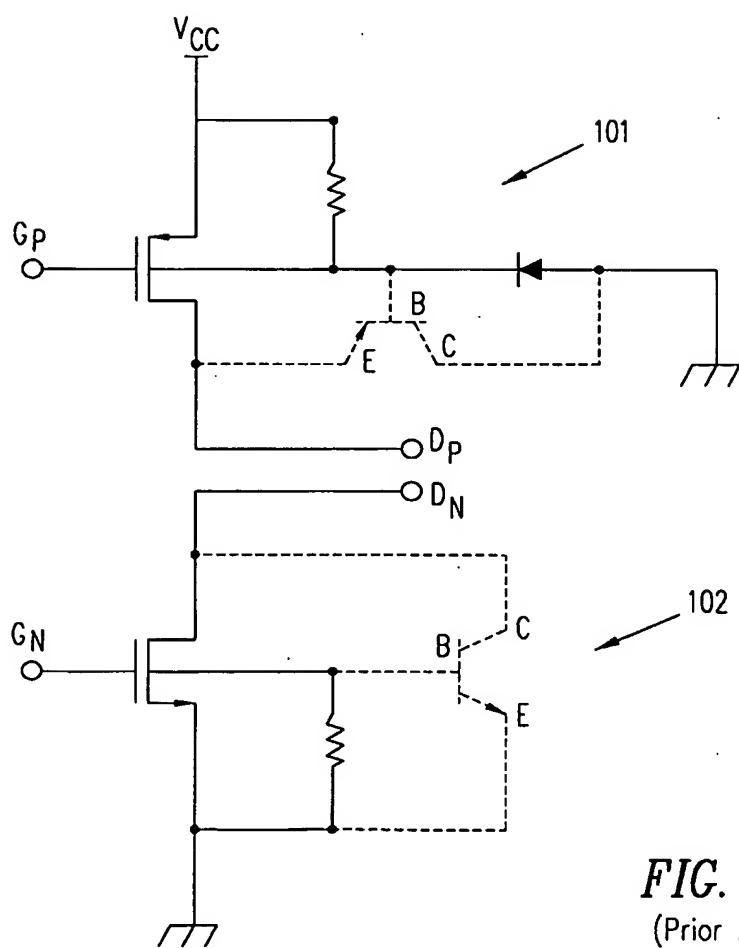


FIG. 1C
(Prior Art)

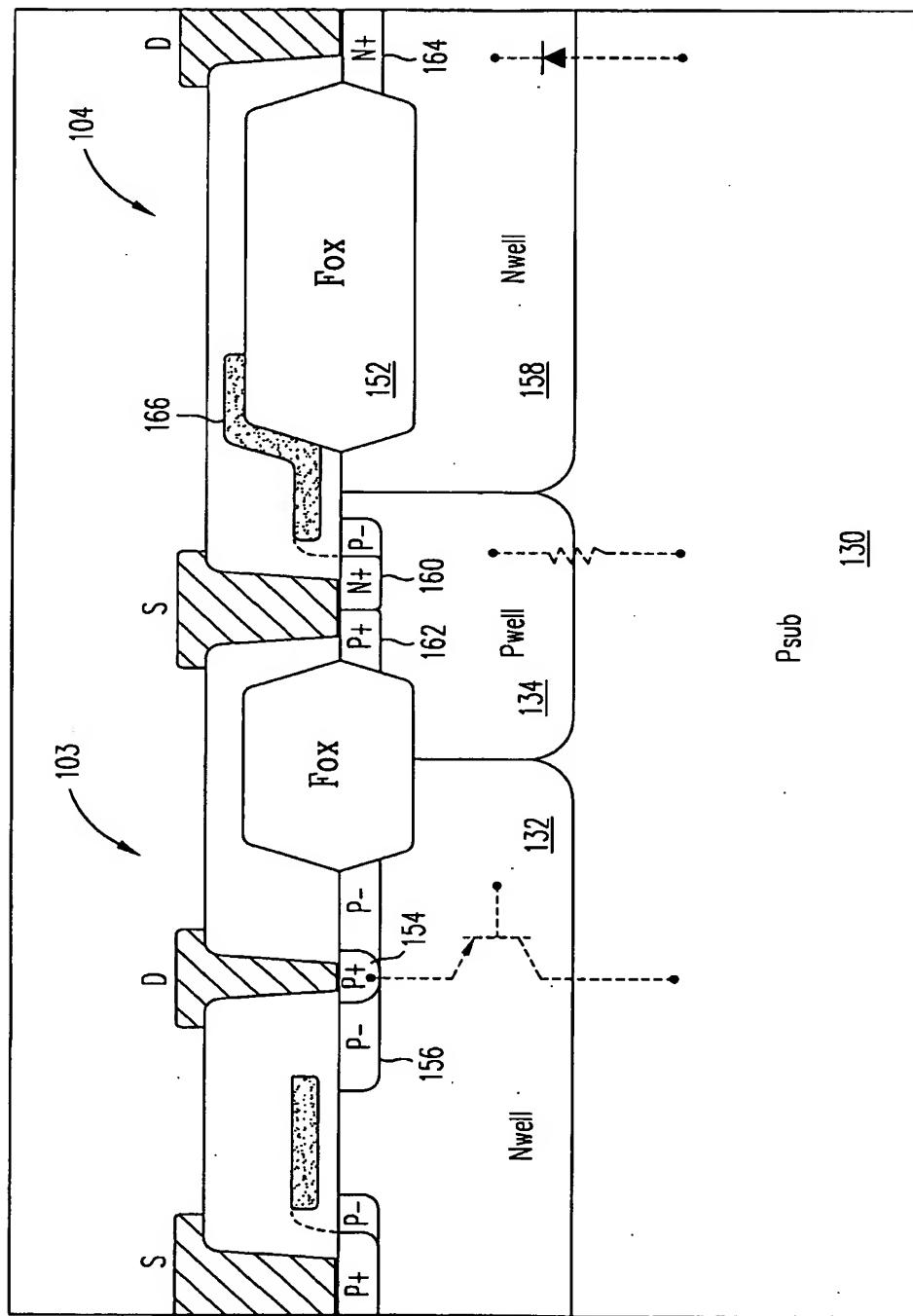
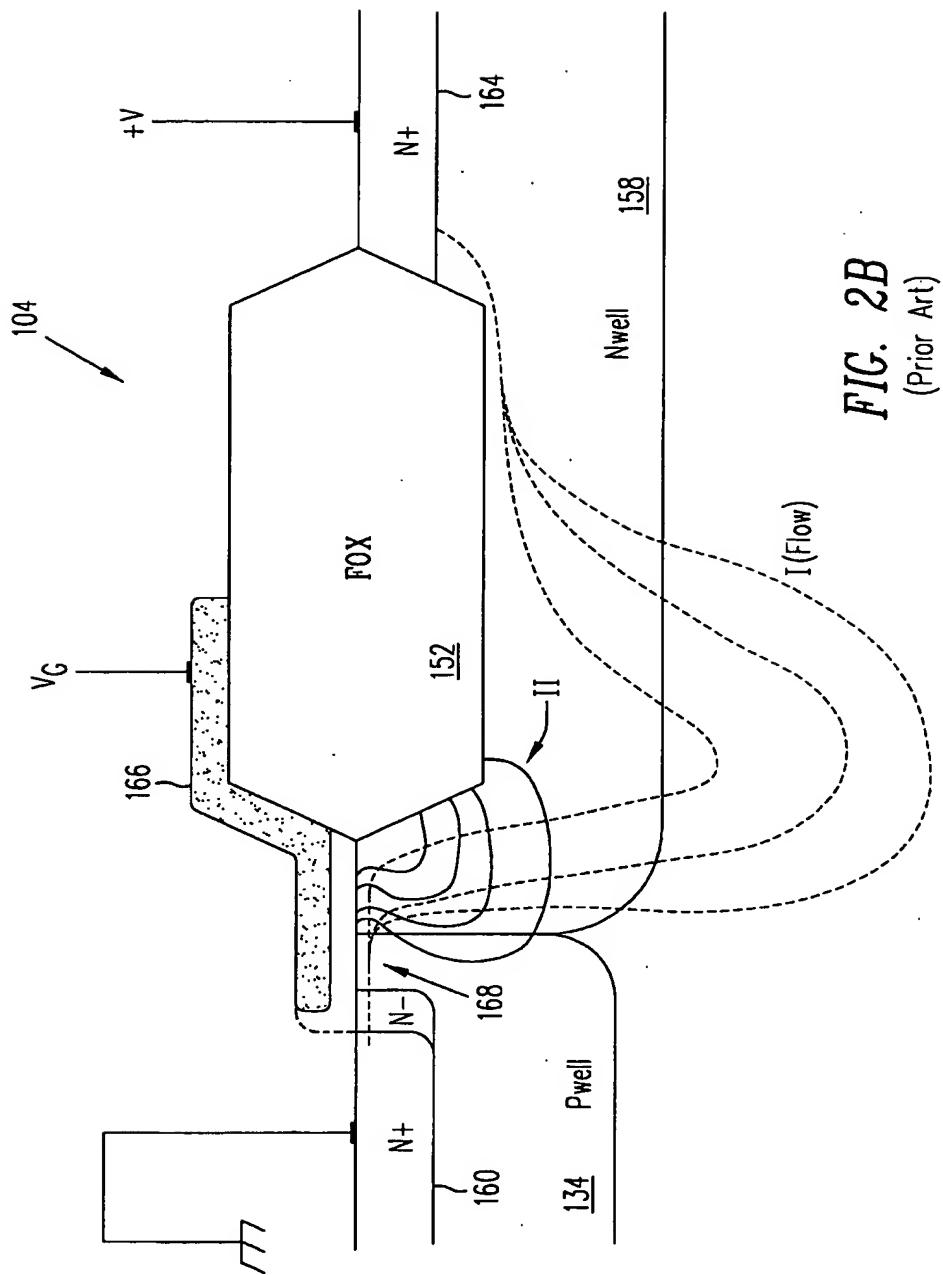


FIG. 2A
(Prior Art)



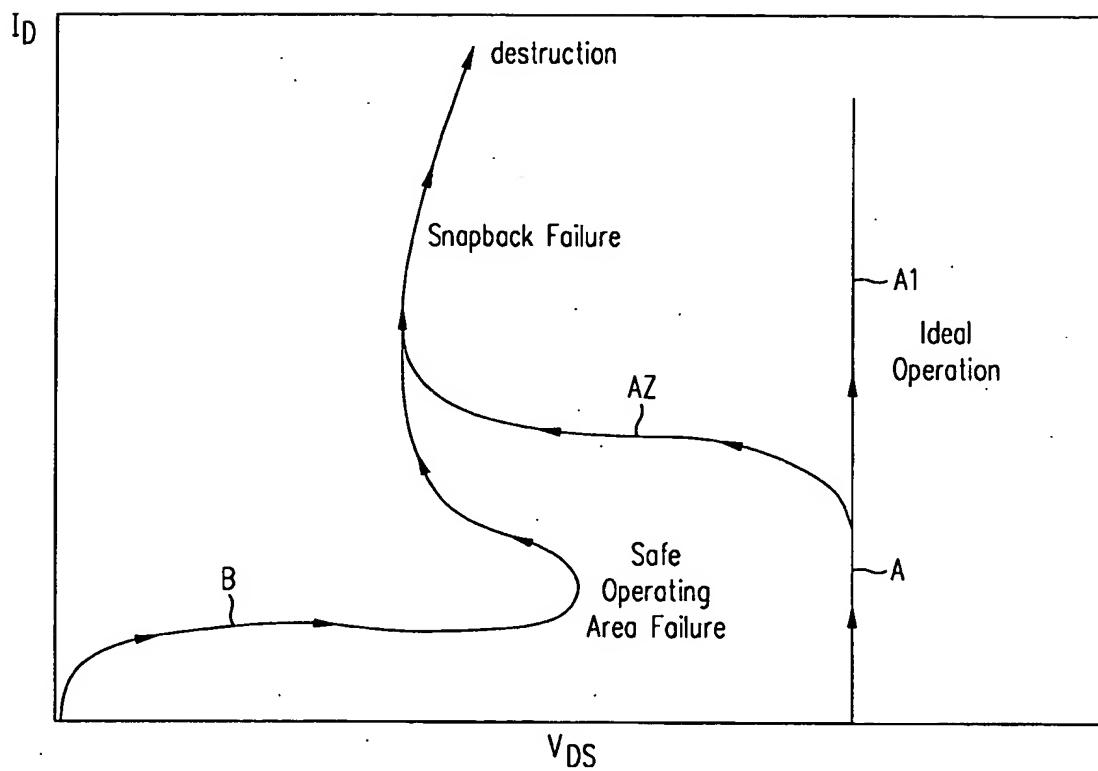
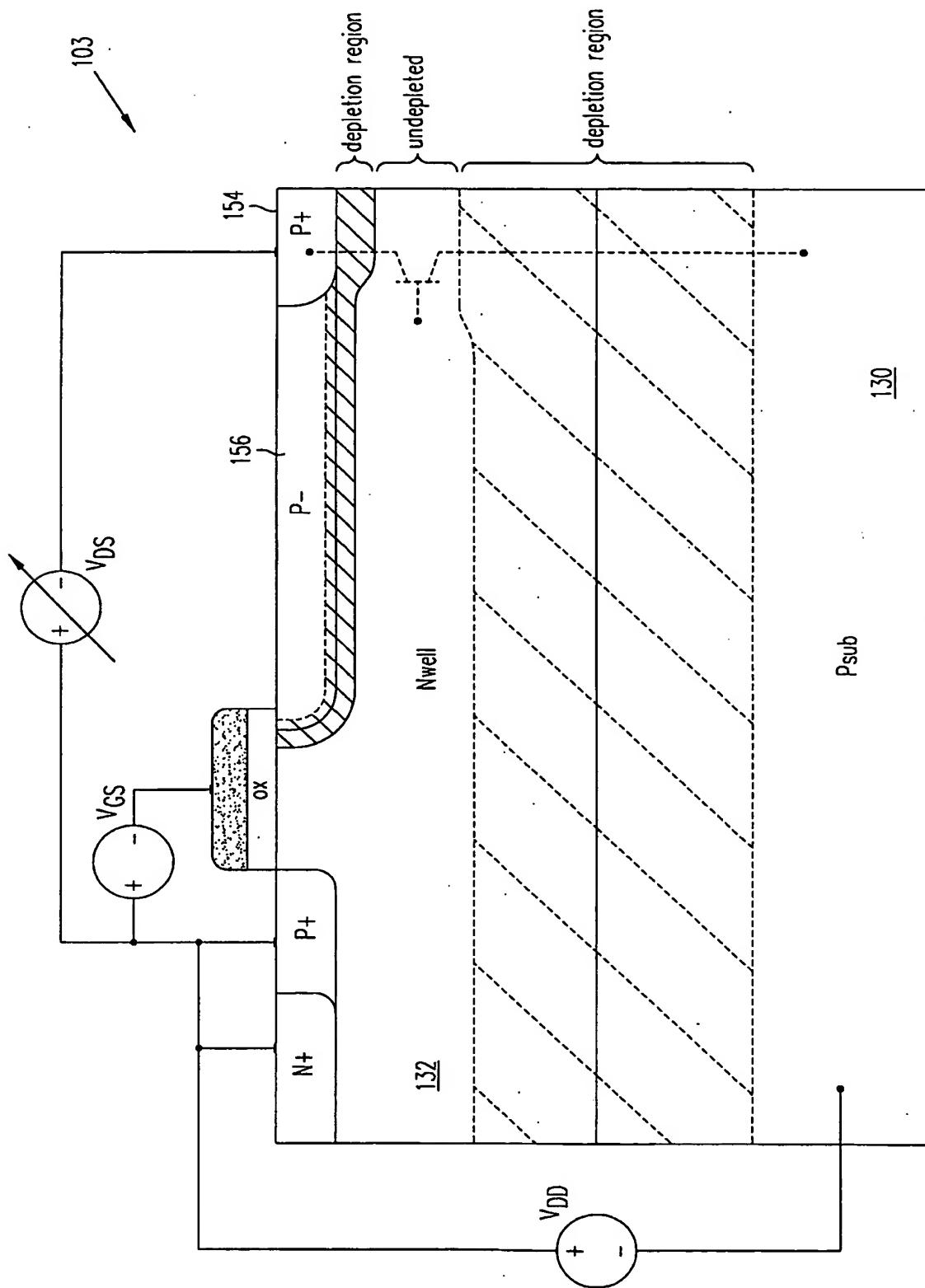


FIG. 2C
(Prior Art)



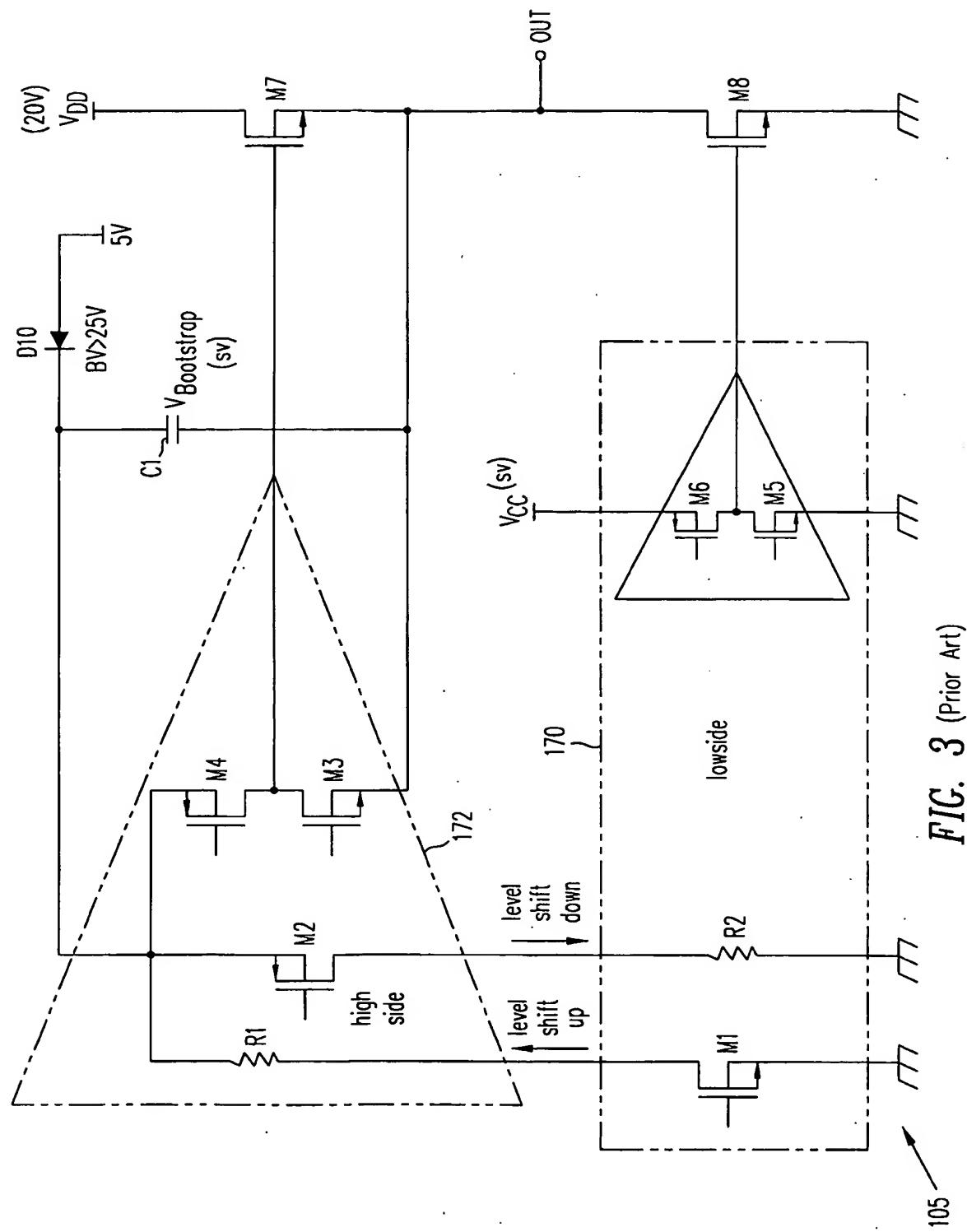


FIG. 3 (Prior Art)

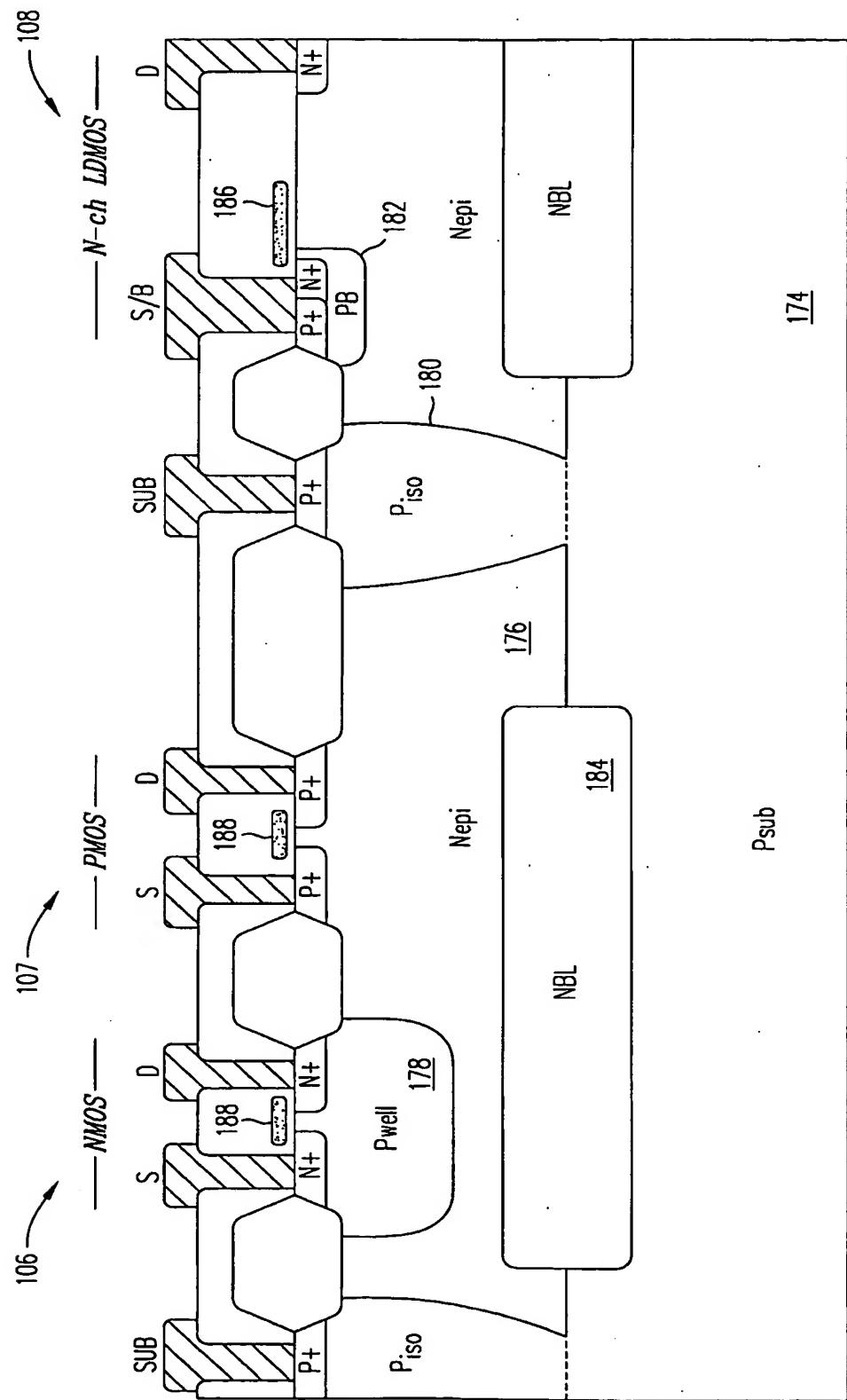


FIG. 4A
(Prior Art)

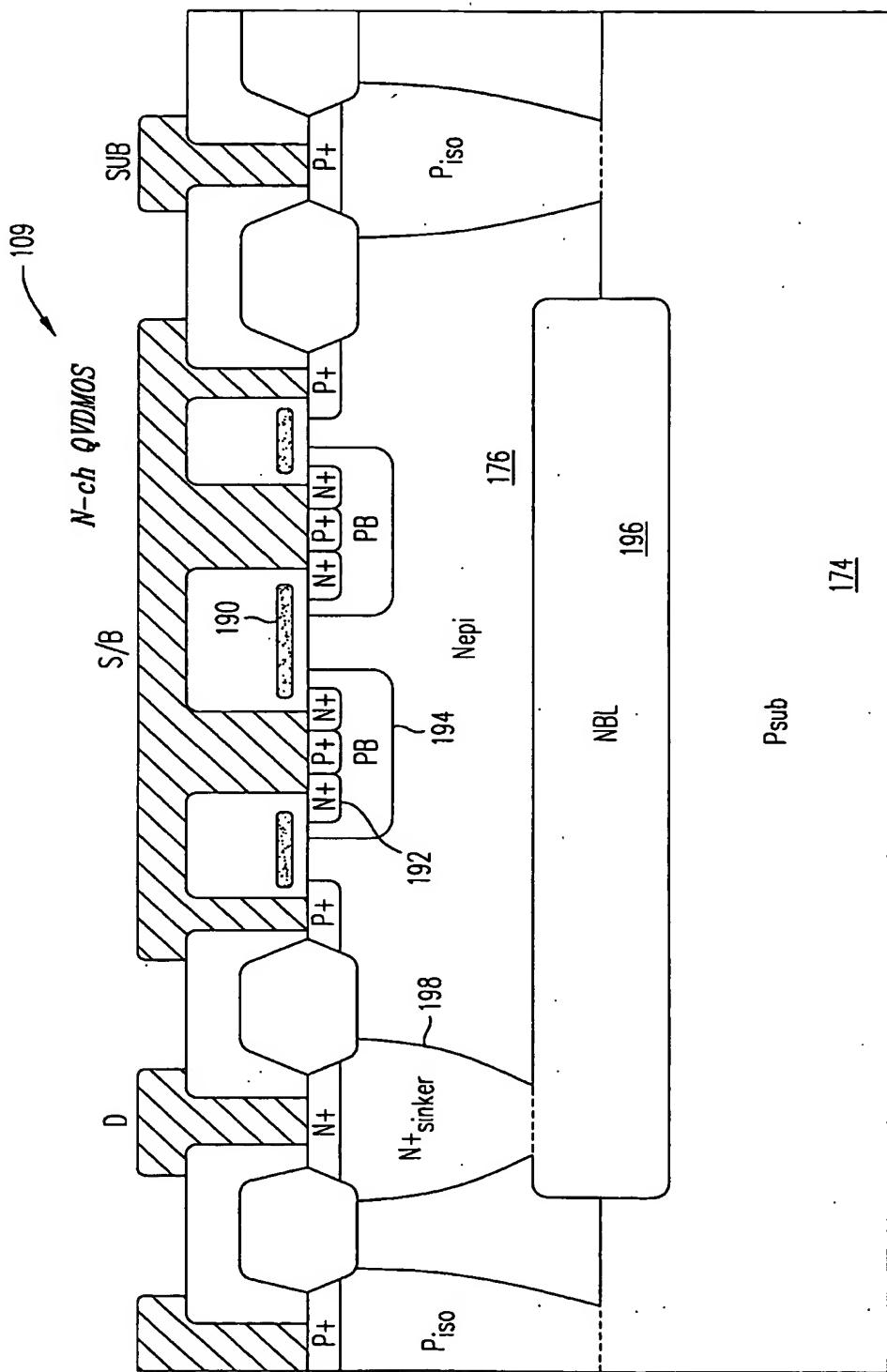


FIG. 4B
(Prior Art)

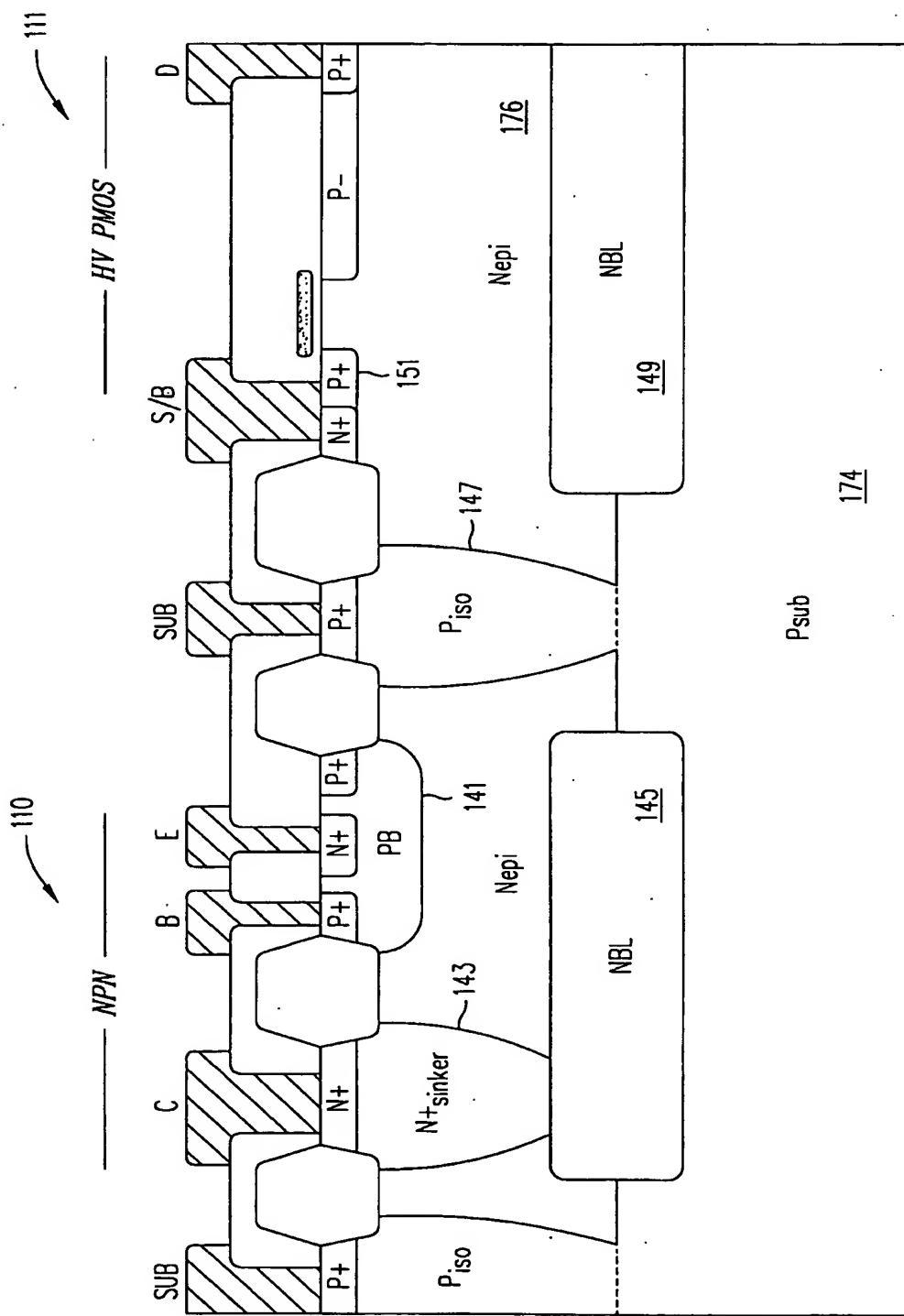


FIG. 4C
(Prior Art)

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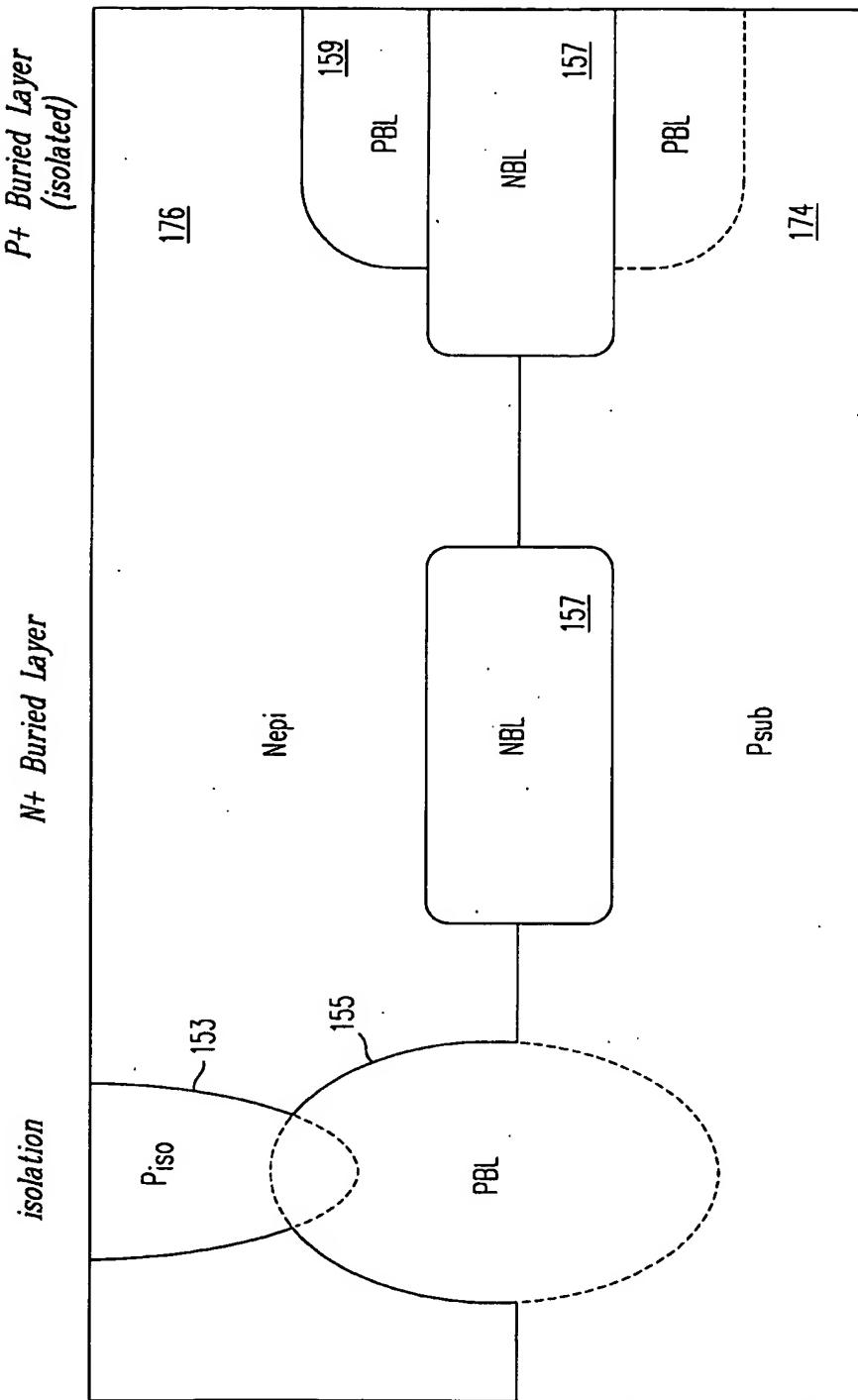


FIG. 5A
(Prior Art)

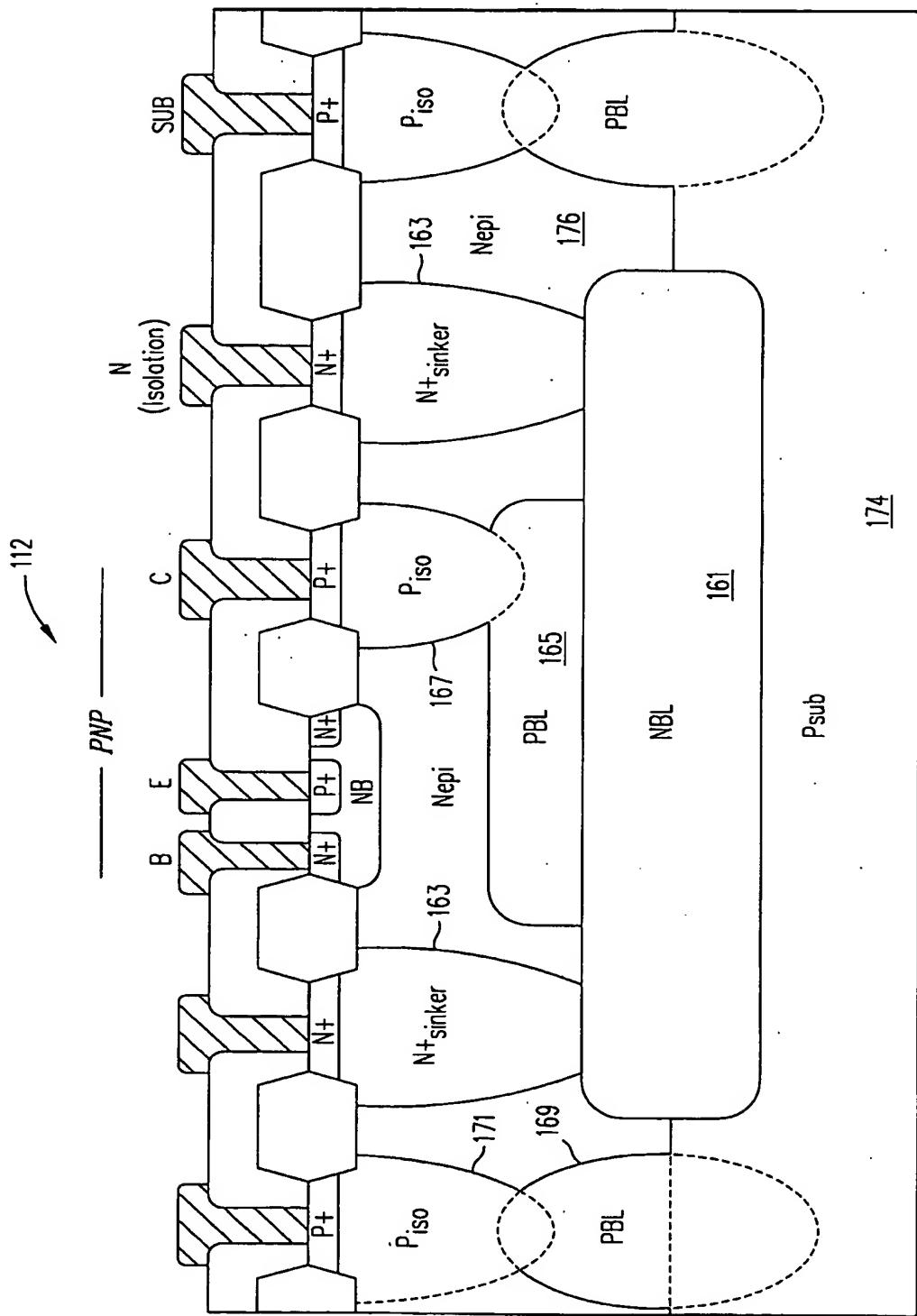


FIG. 5B
(Prior Art)

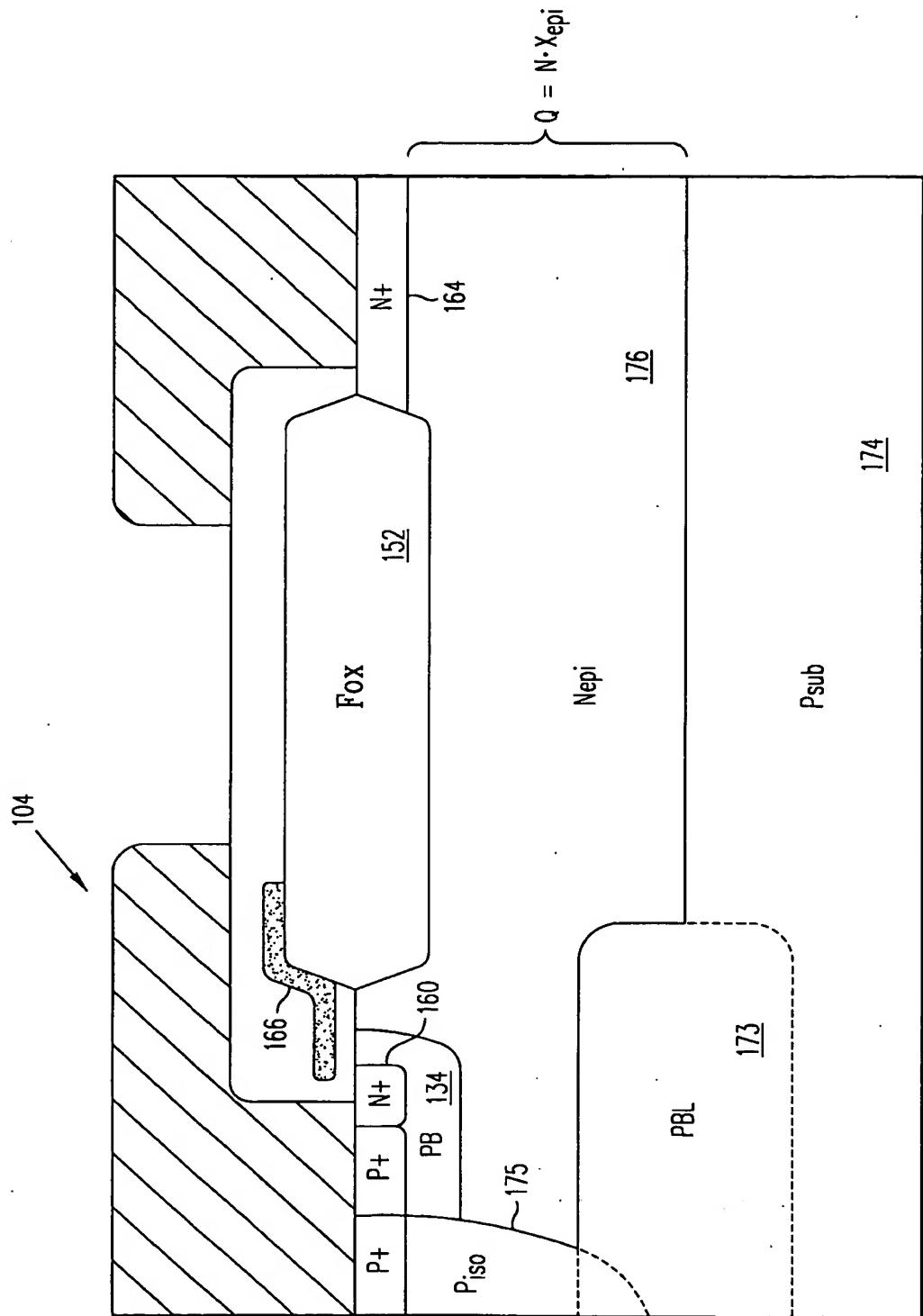


FIG. 5C
(Prior Art)

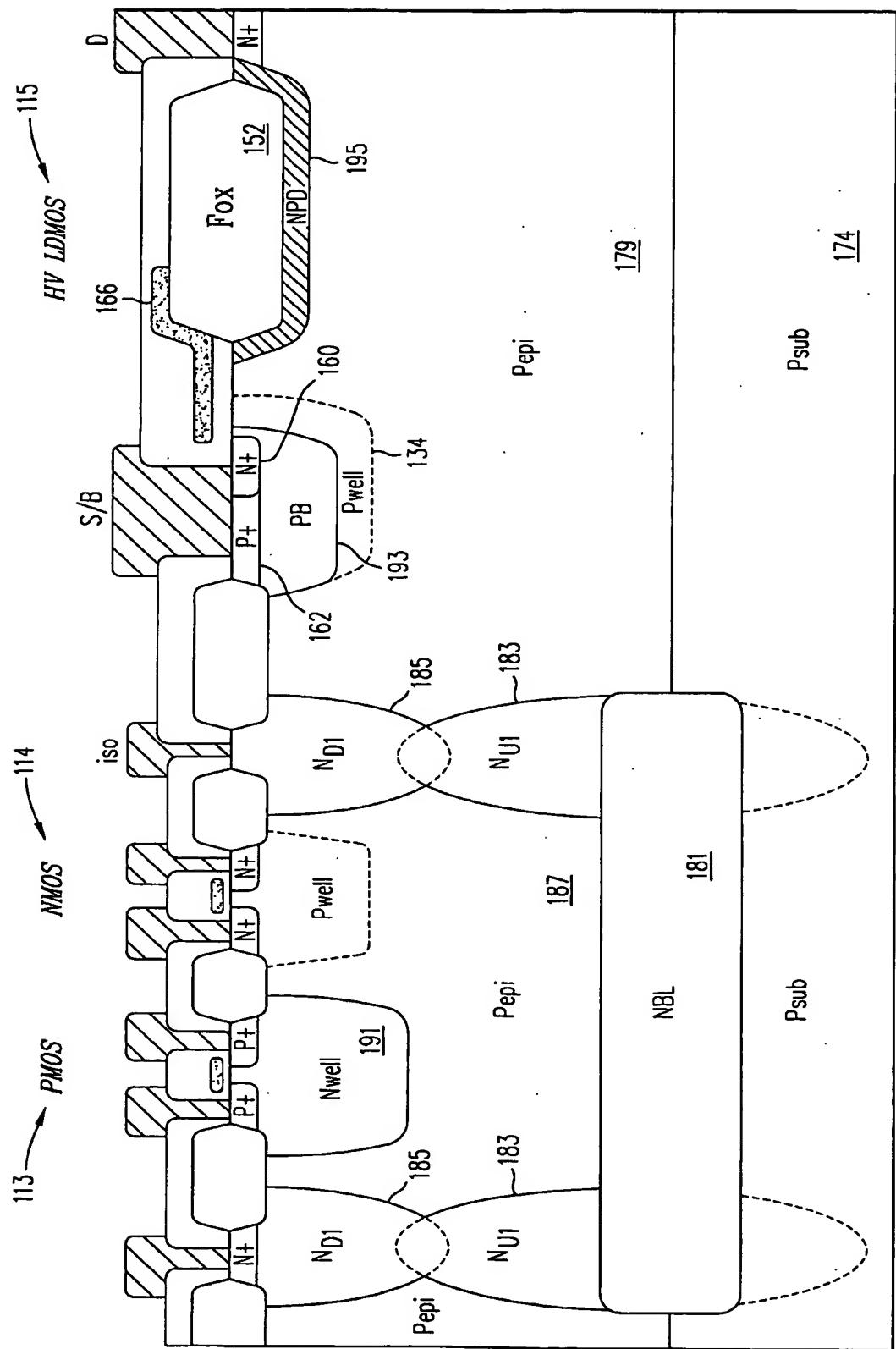


FIG. 6A (Prior Art)

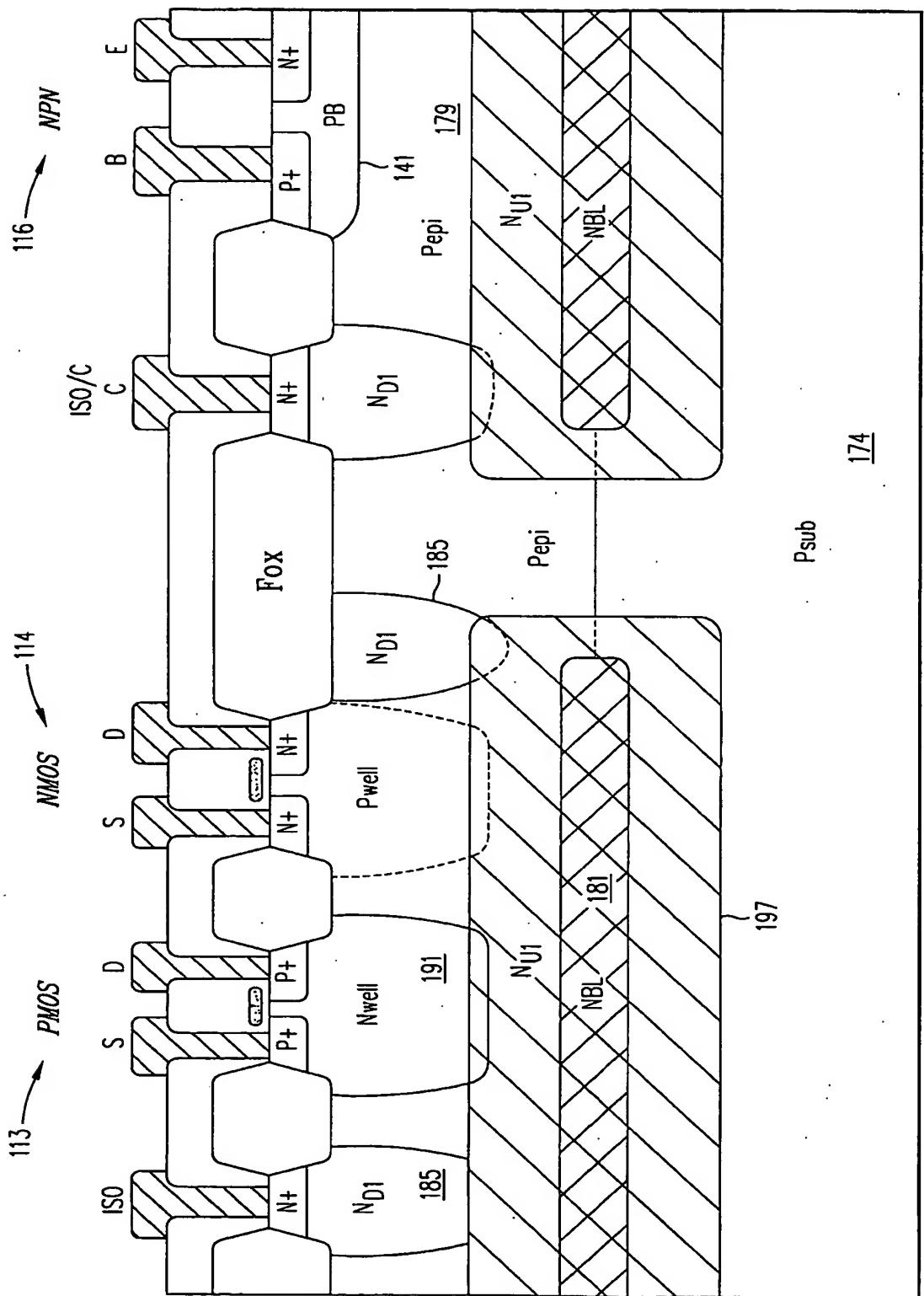


FIG. 6B (Prior Art)

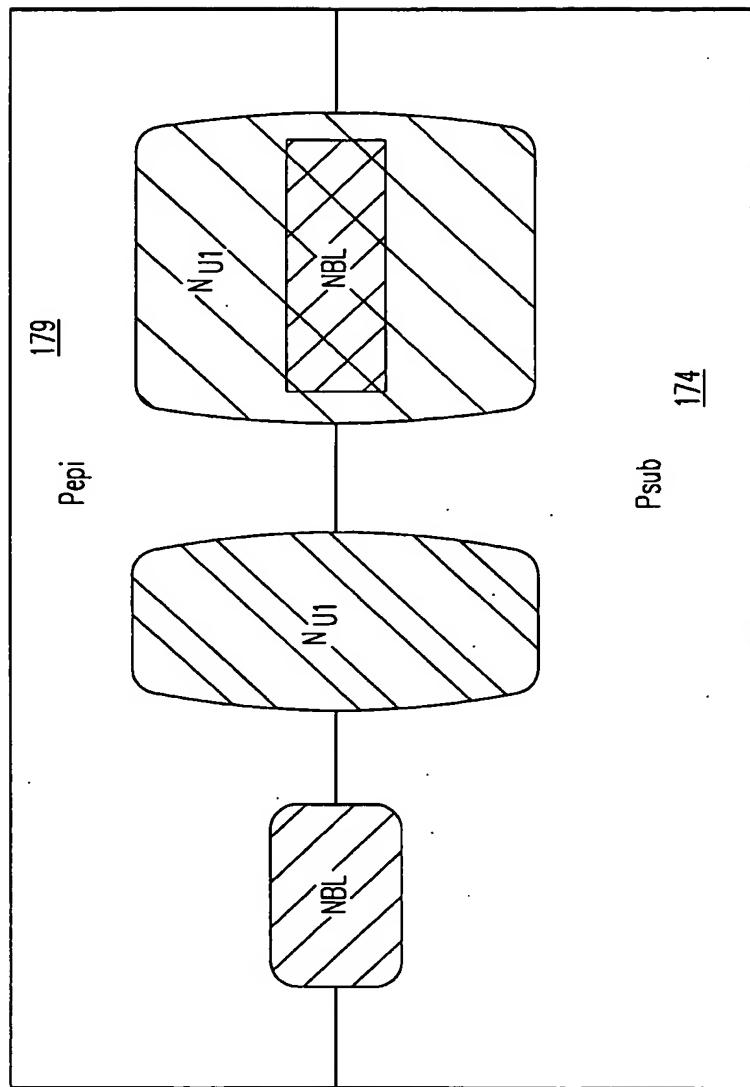


FIG. 6C
(Prior Art)

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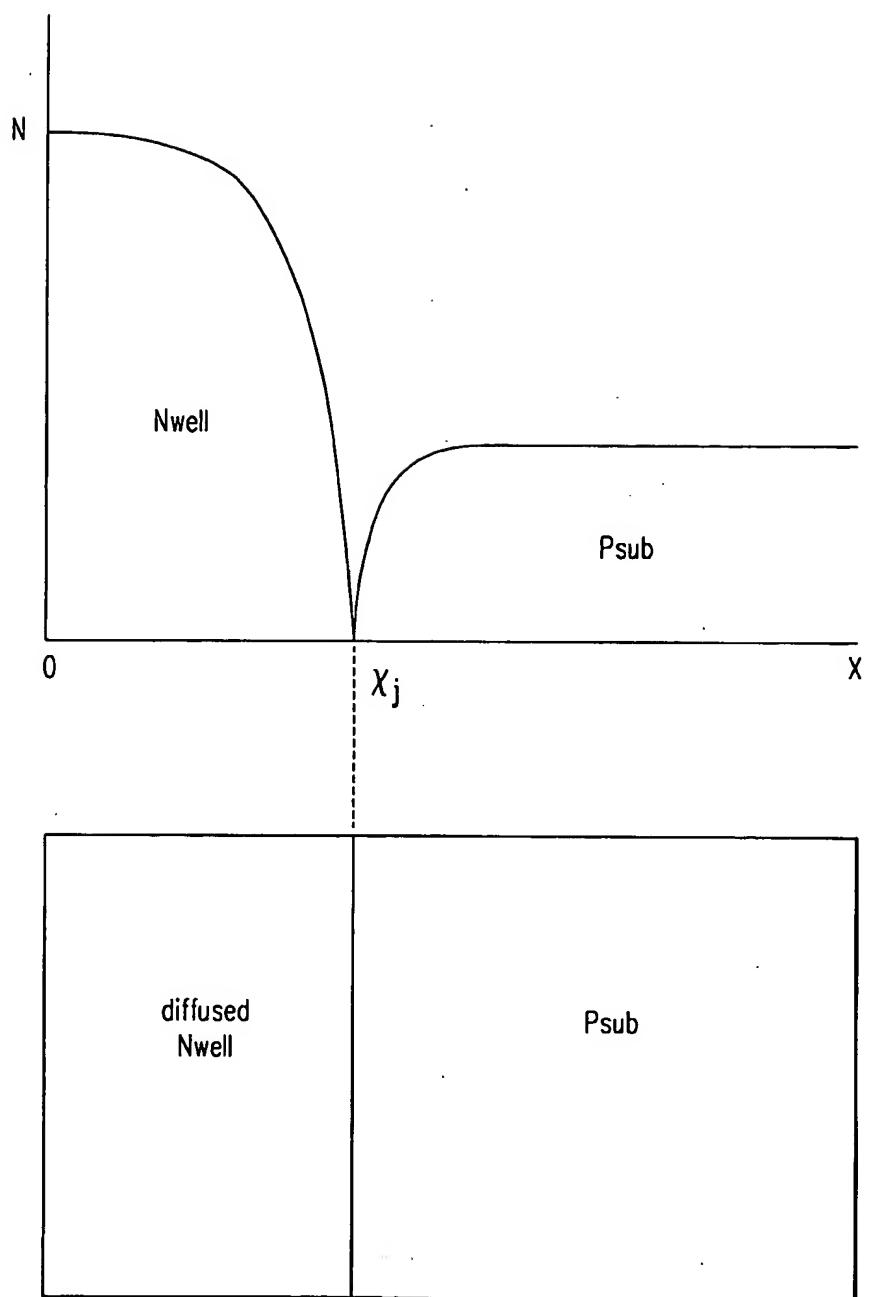


FIG. 7A
(Prior Art)

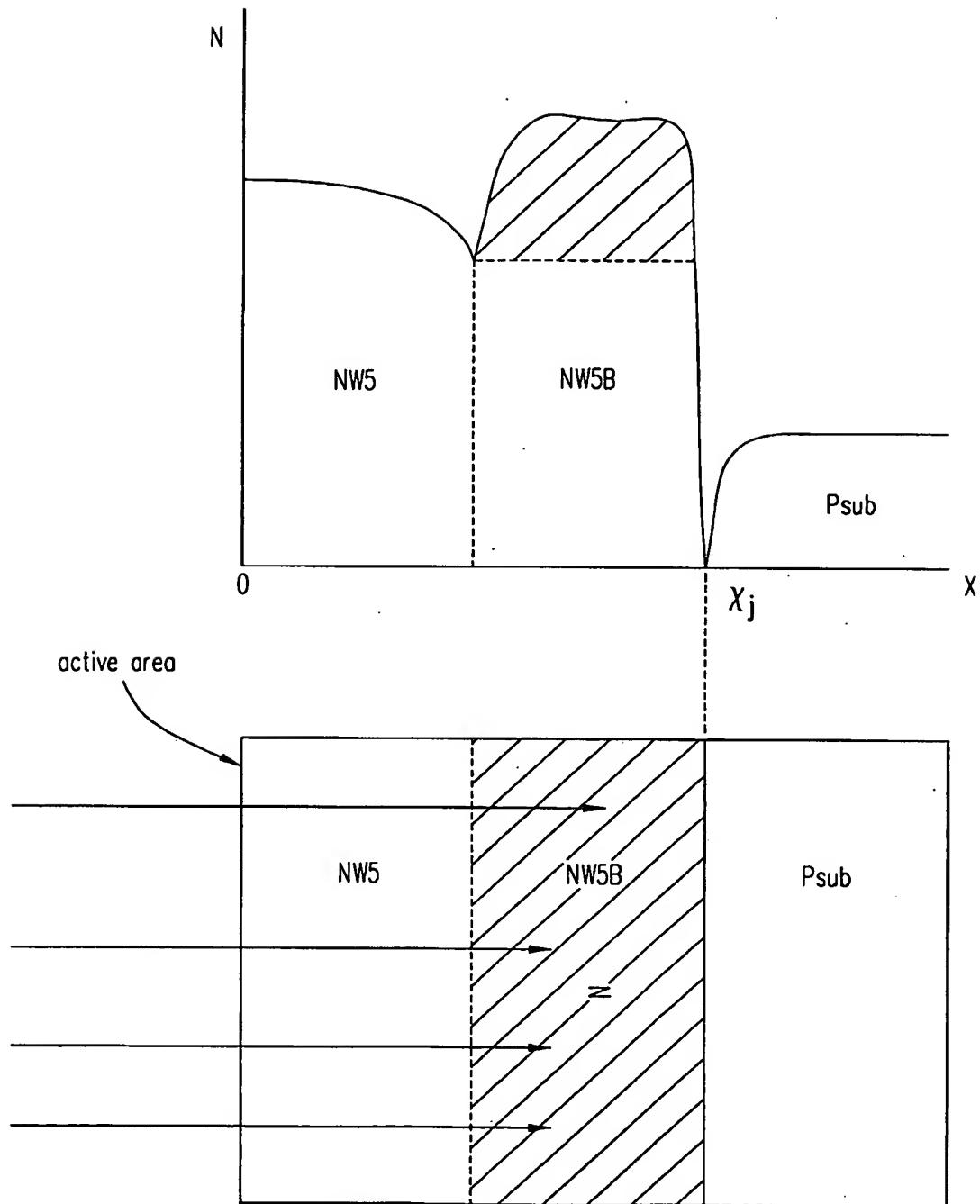


FIG. 7B

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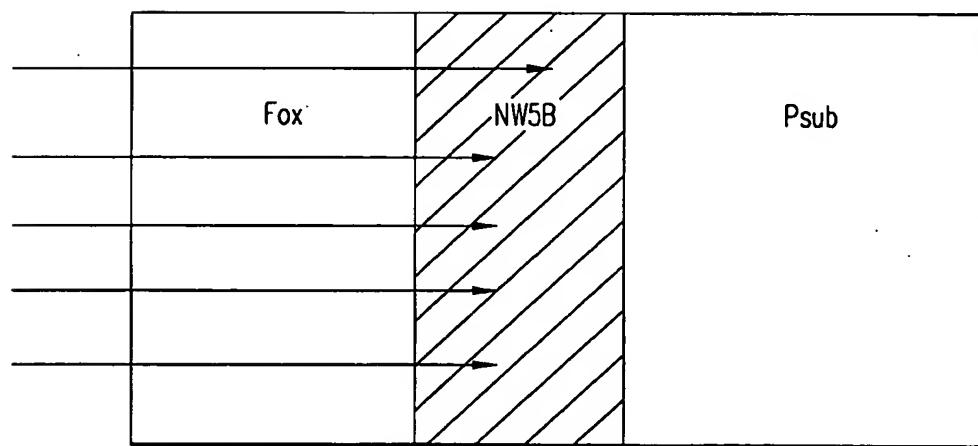
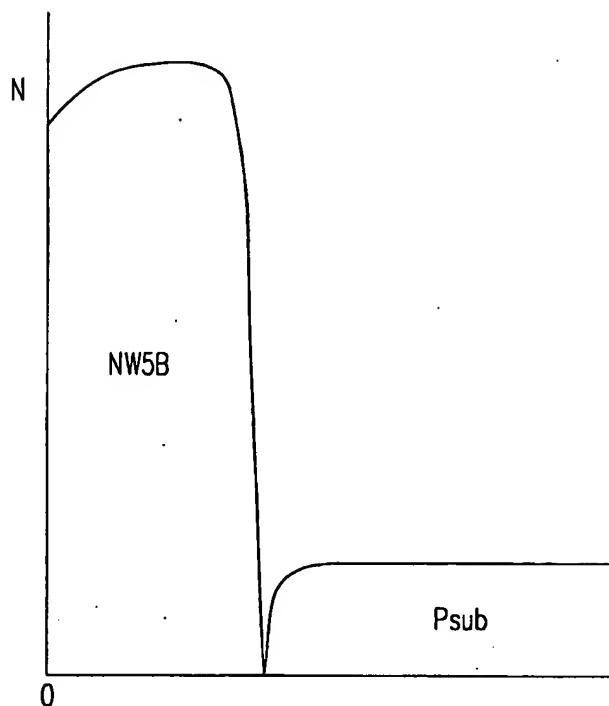


FIG. 7C

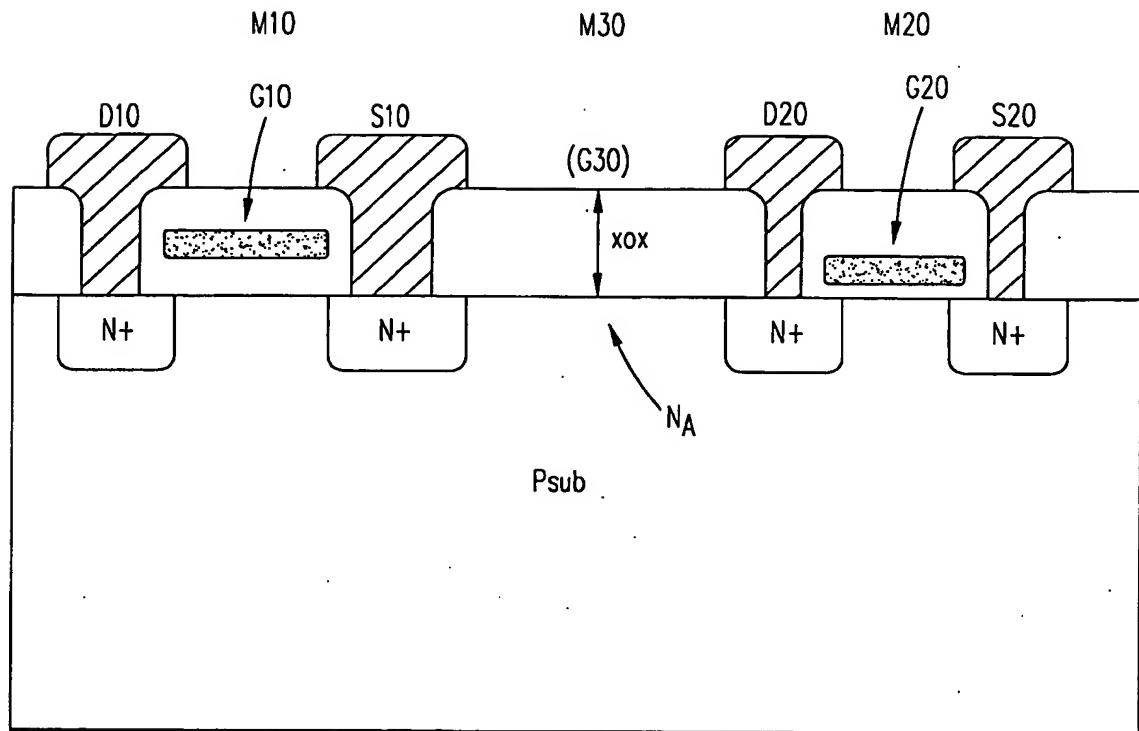


FIG. 8A

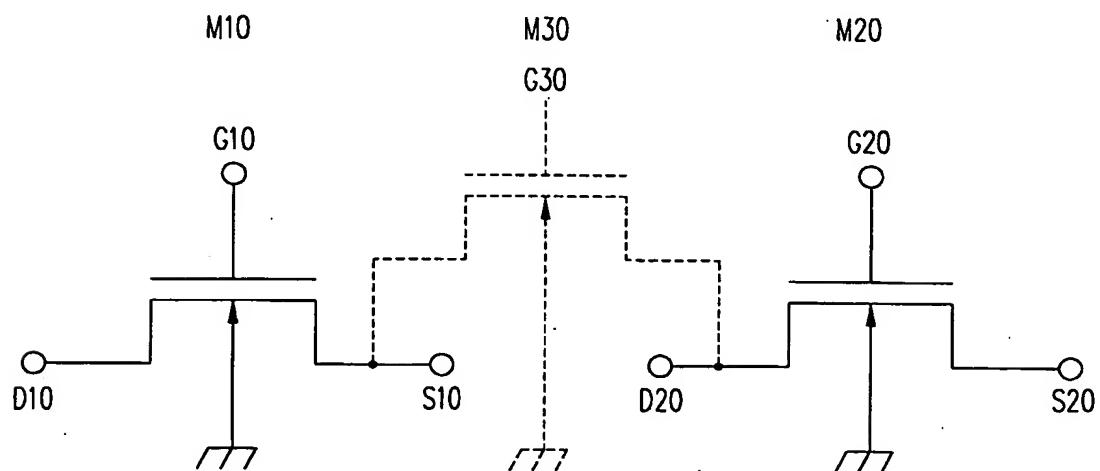


FIG. 8B

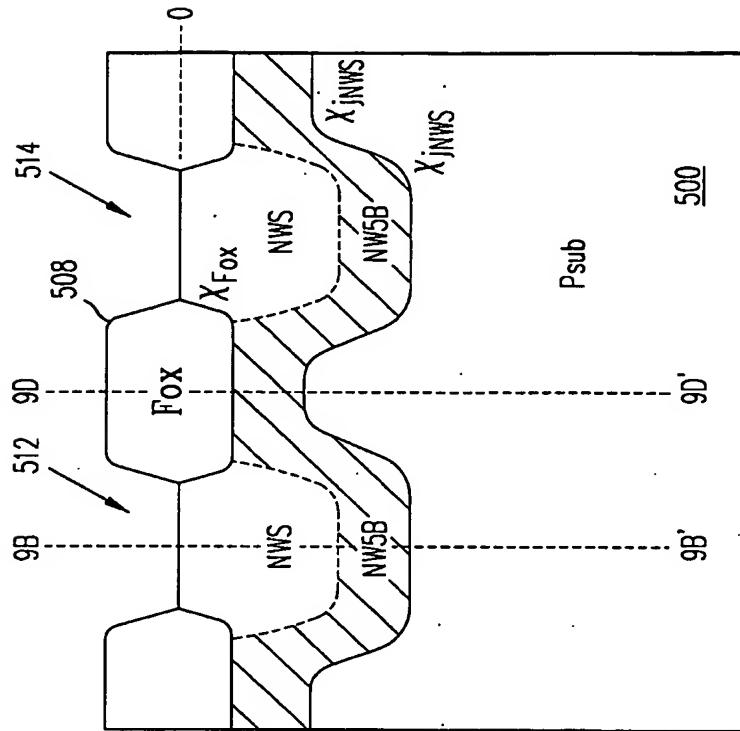


FIG. 9B

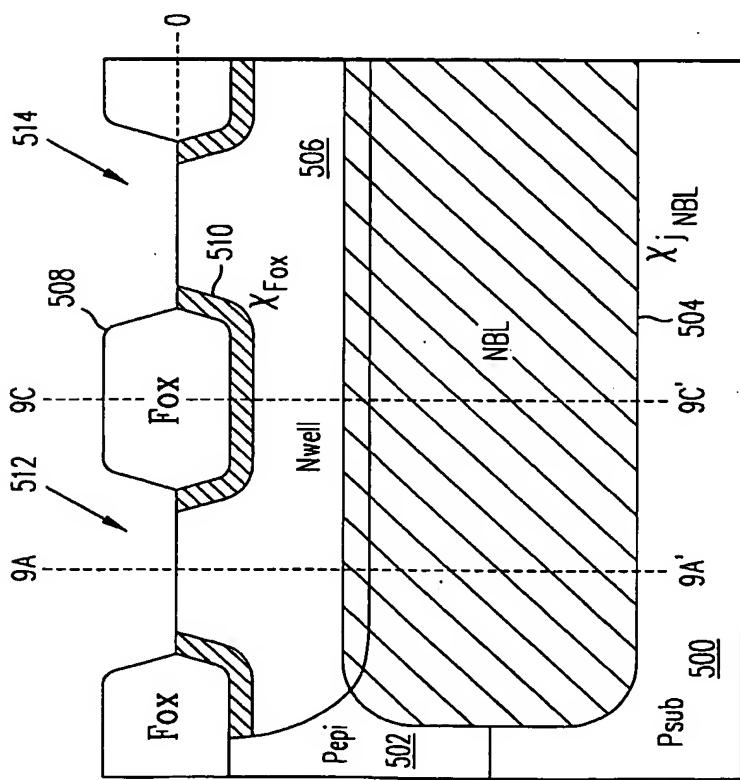


FIG. 9A
(Prior Art)

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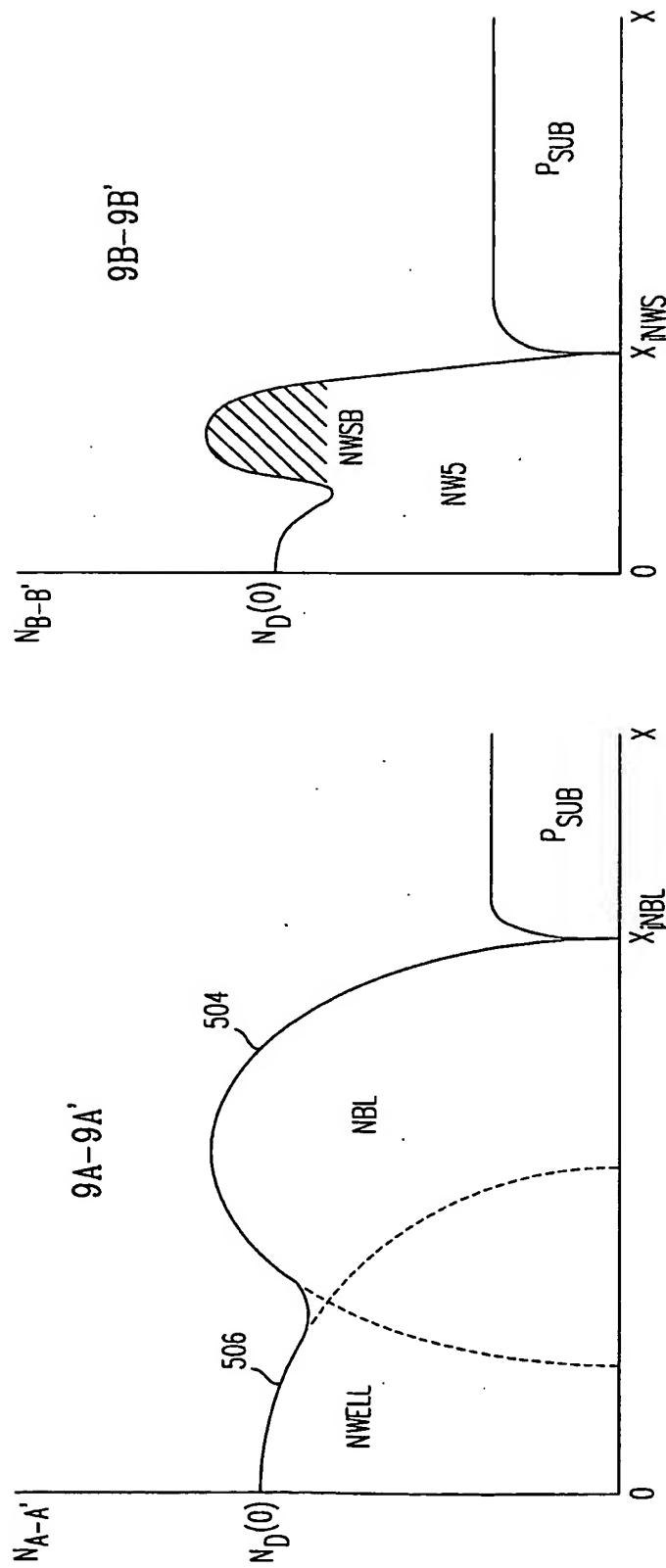


FIG. 9D
(Prior Art)

FIG. 9C
(Prior Art)

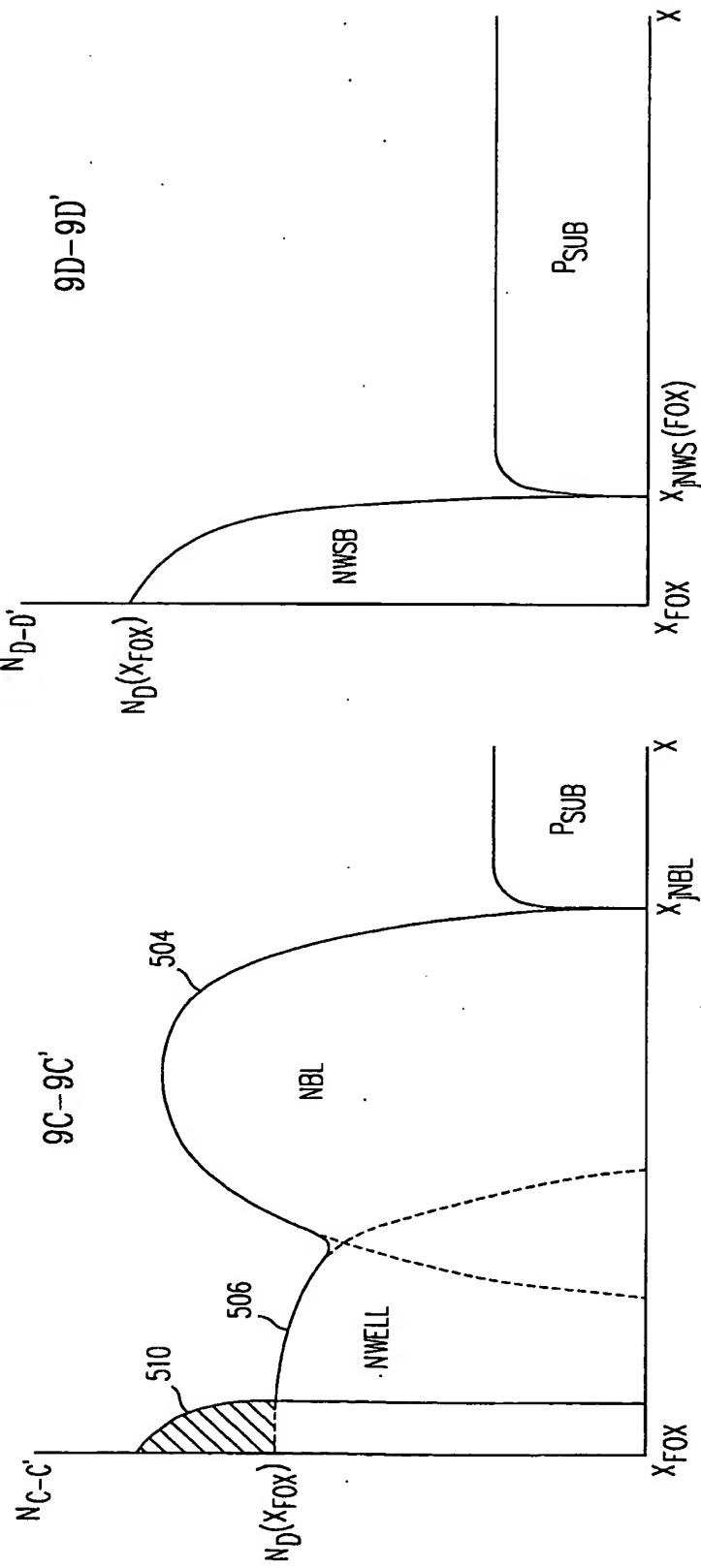


FIG. 9F
(Prior Art)

FIG. 9E
(Prior Art)

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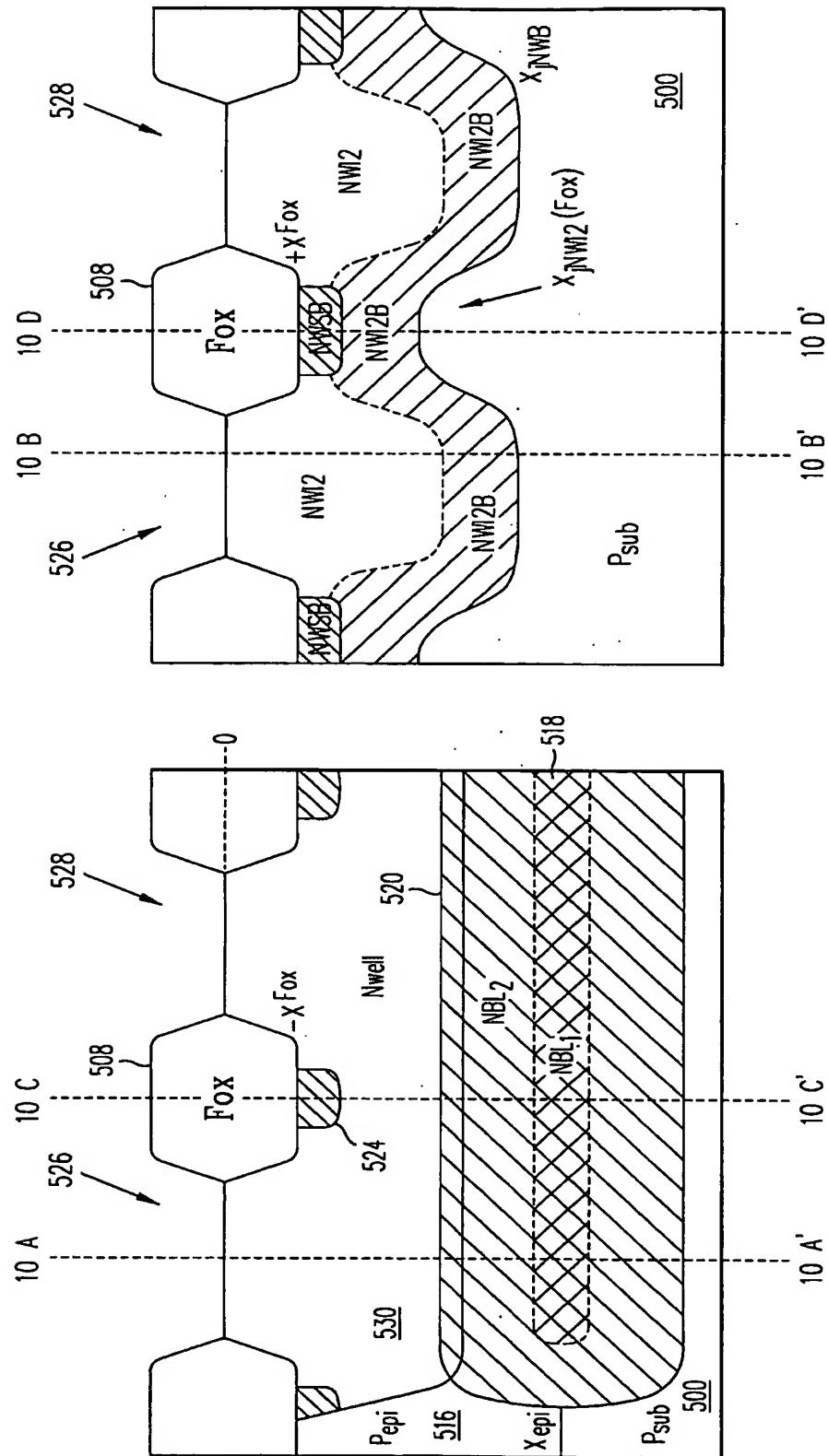


FIG. 10A
(Prior Art)

FIG. 10B

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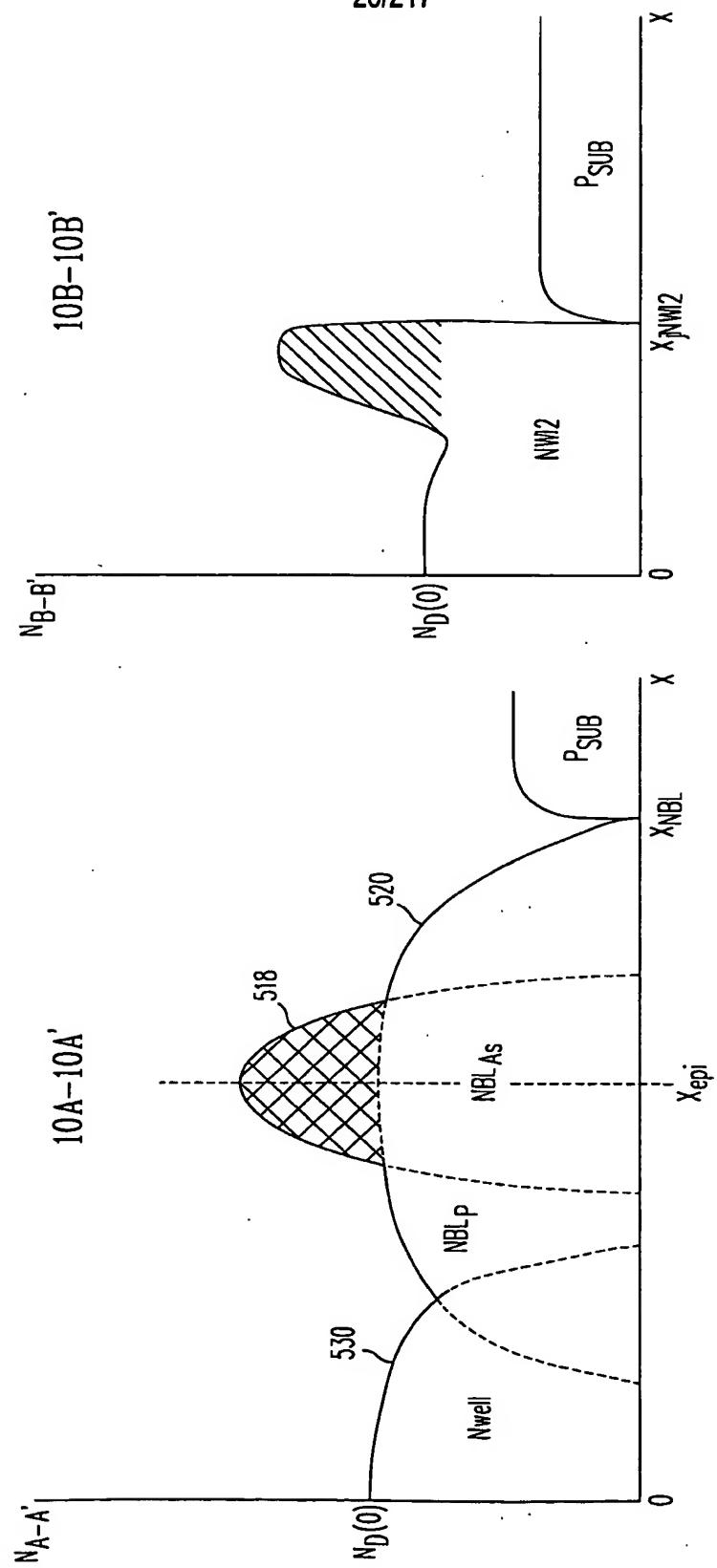


FIG. 10C
(Prior Art)
FIG. 10D

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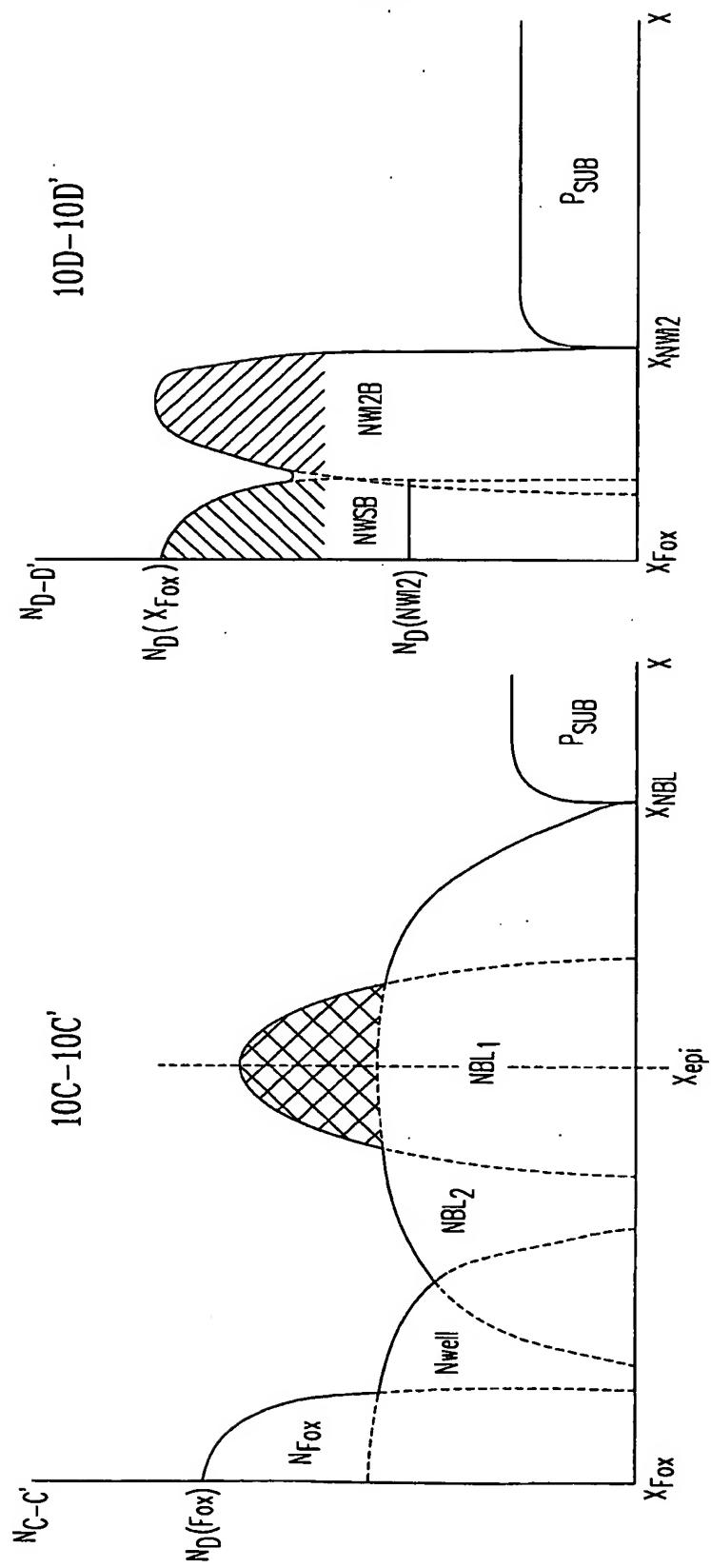


FIG. 10E
(Prior Art)

FIG. 10F

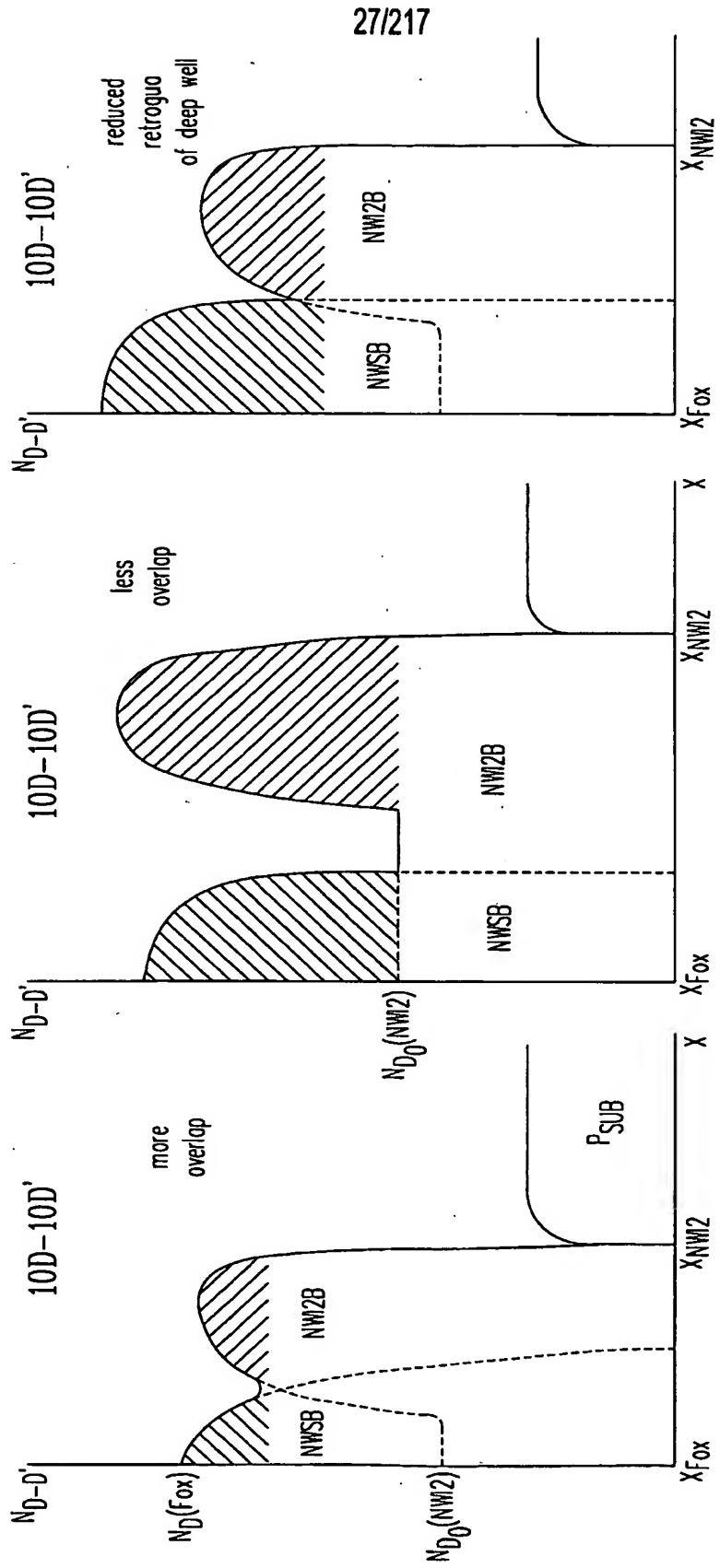


FIG. 10H

FIG. 10I

FIG. 10G

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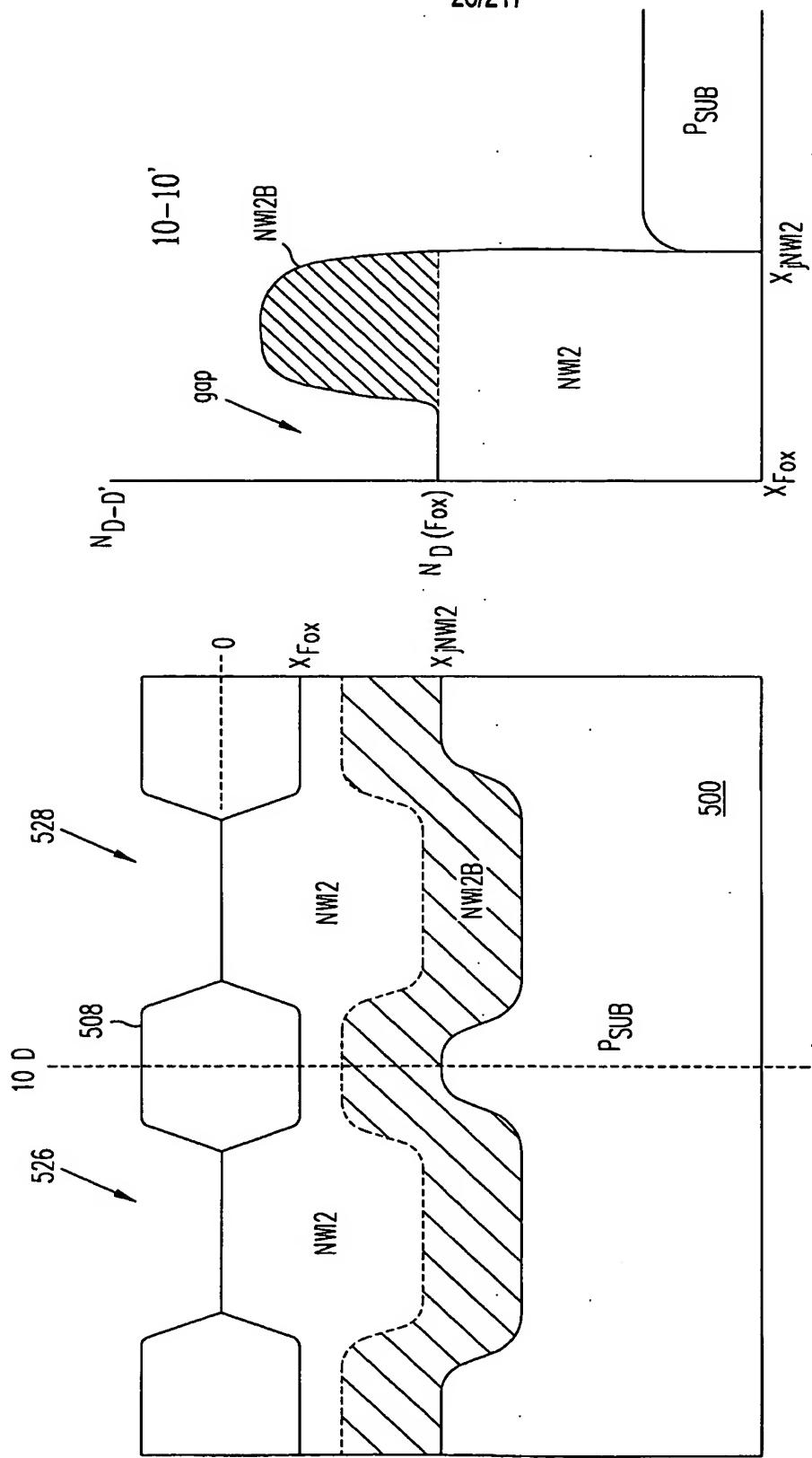
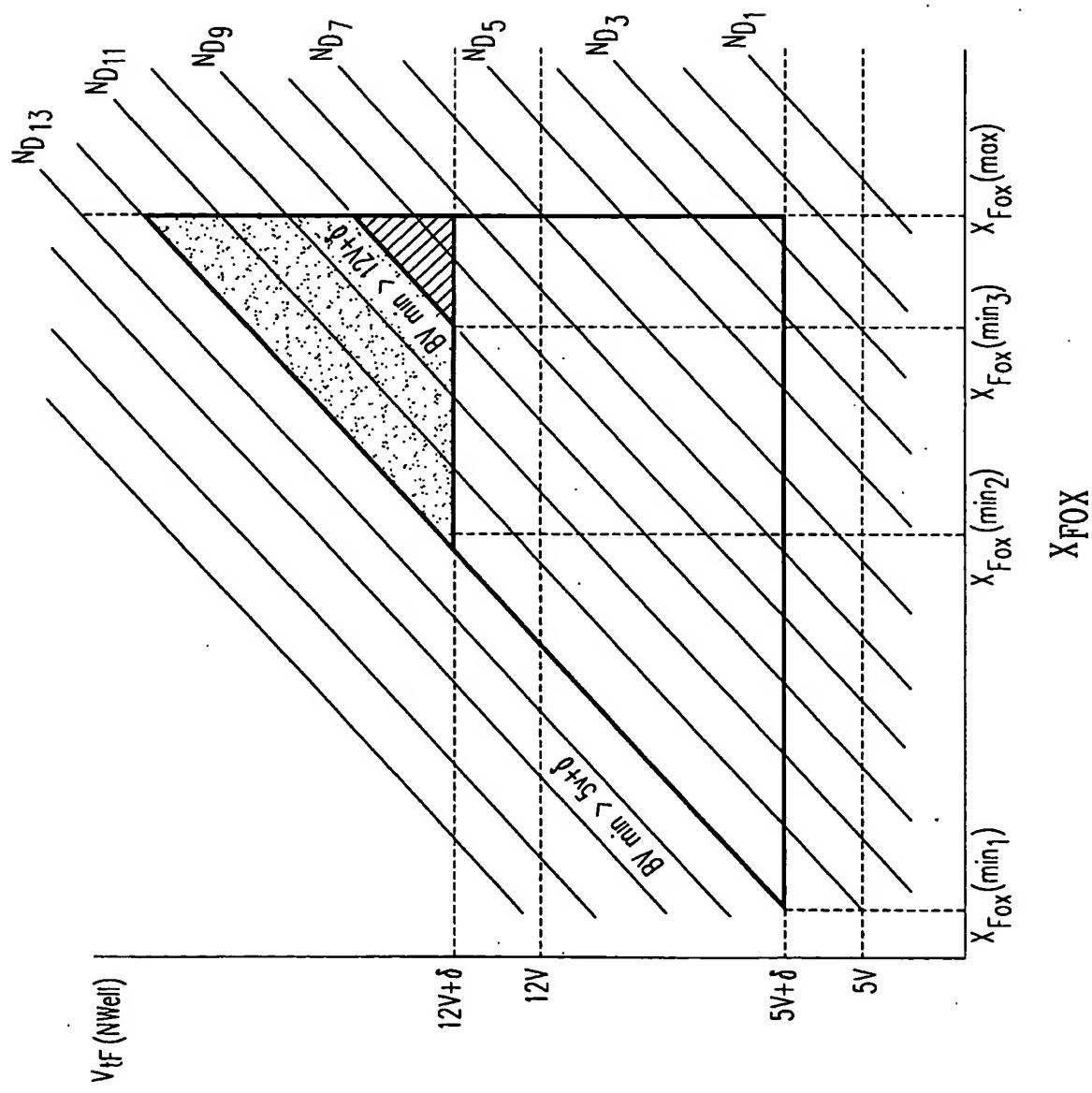


FIG. 10K

FIG. 10J



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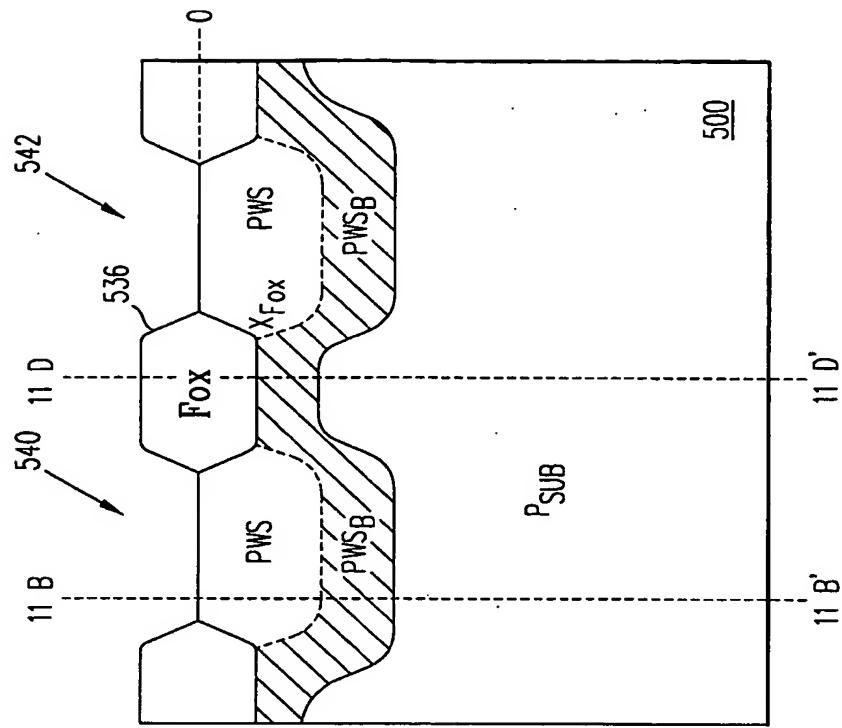


FIG. 11B

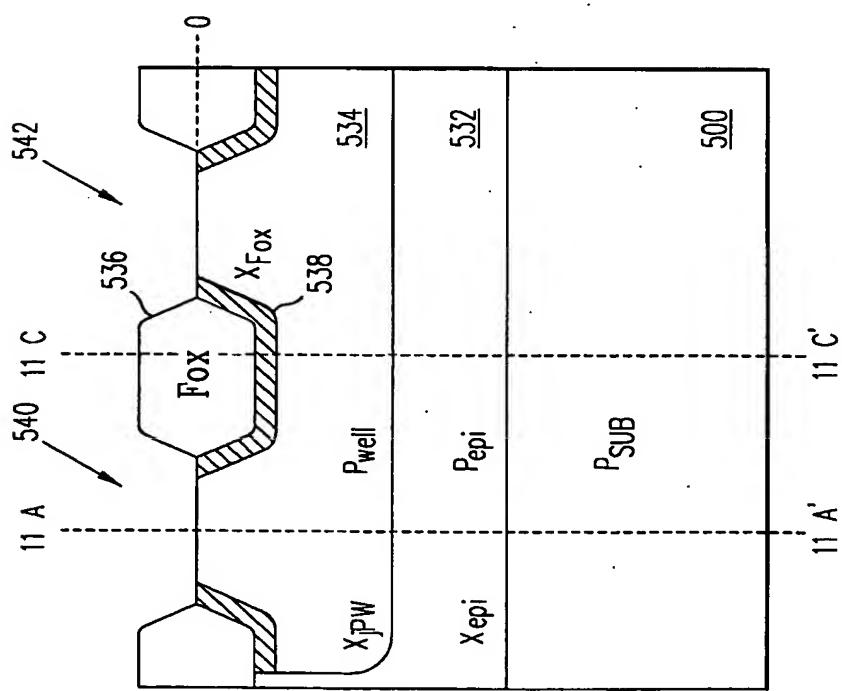


FIG. 11A

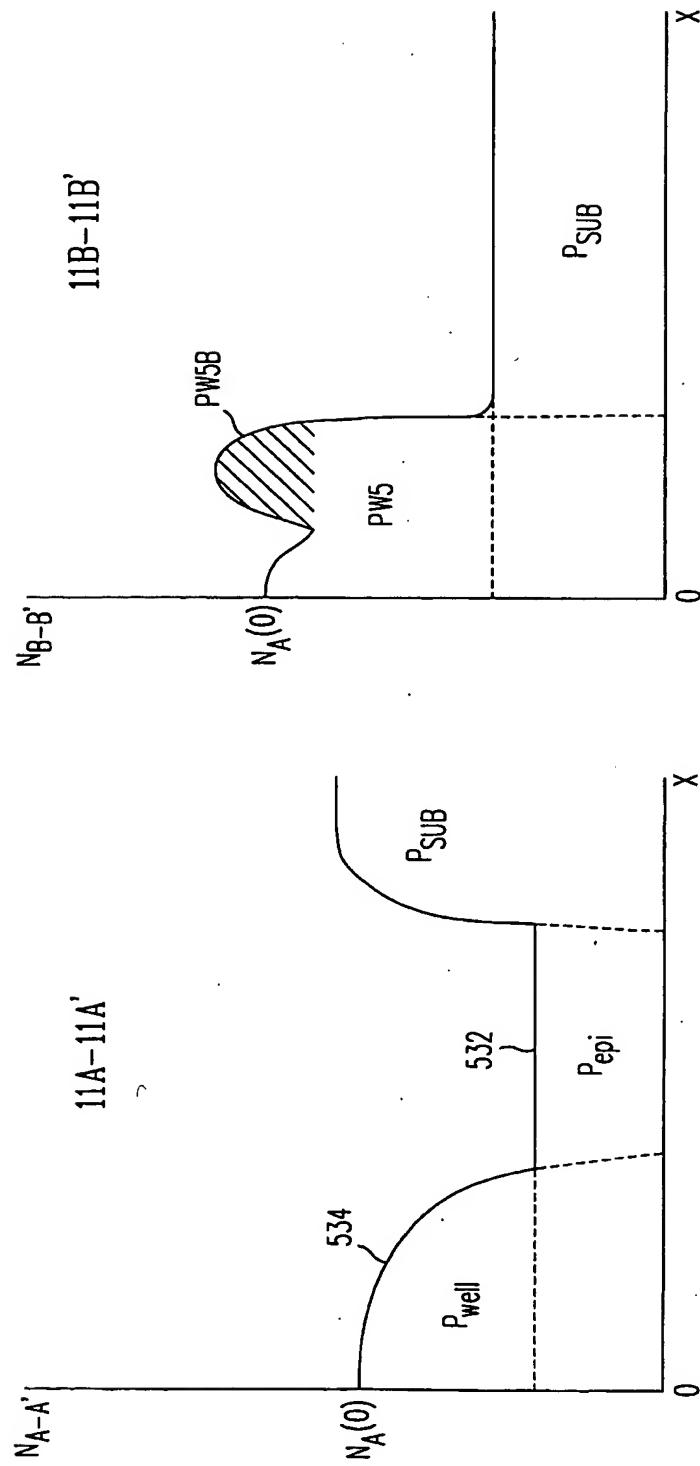


FIG. 11D

FIG. 11C

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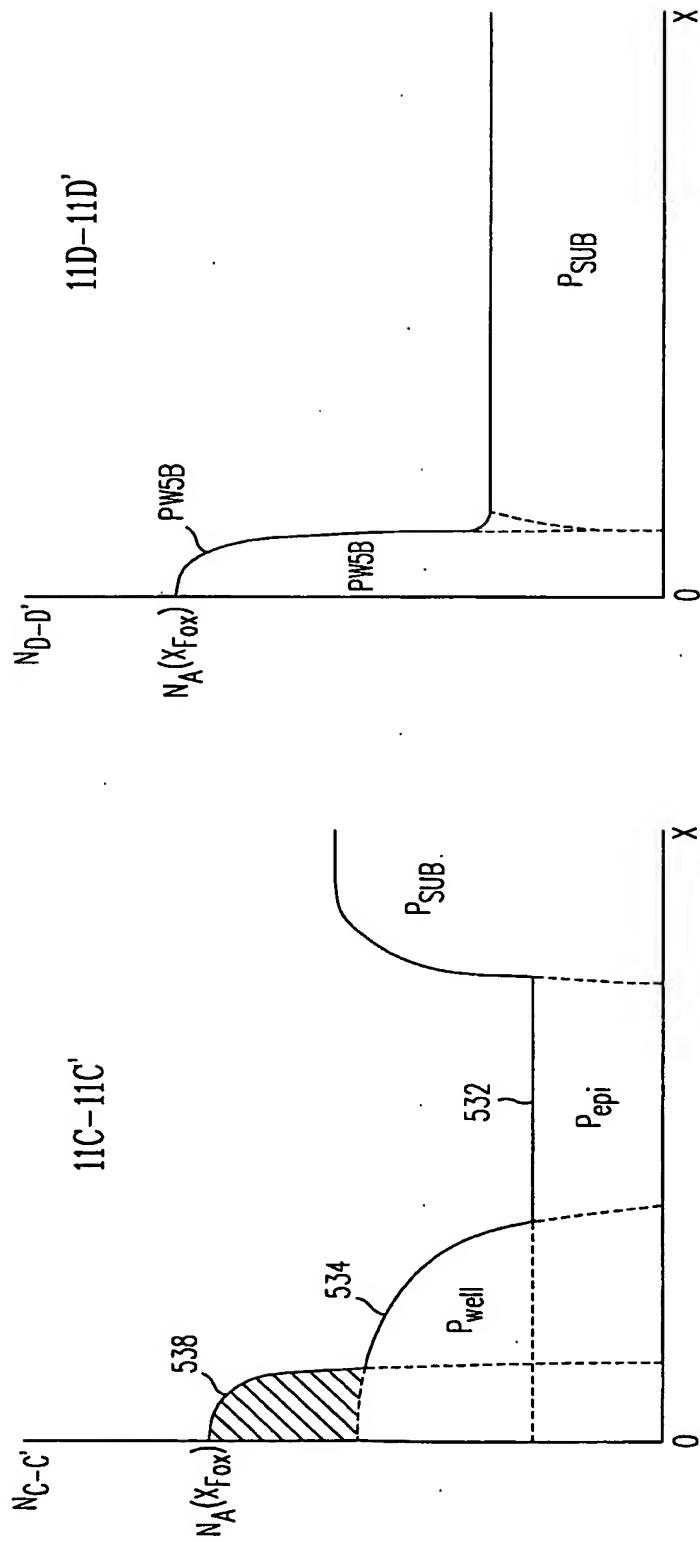


FIG. 11F

FIG. 11E

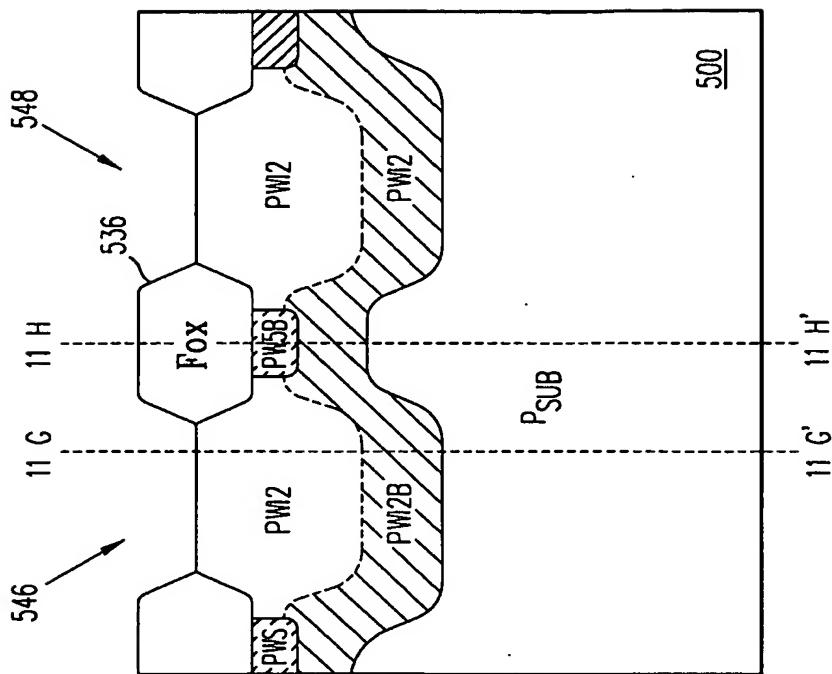


FIG. 11H

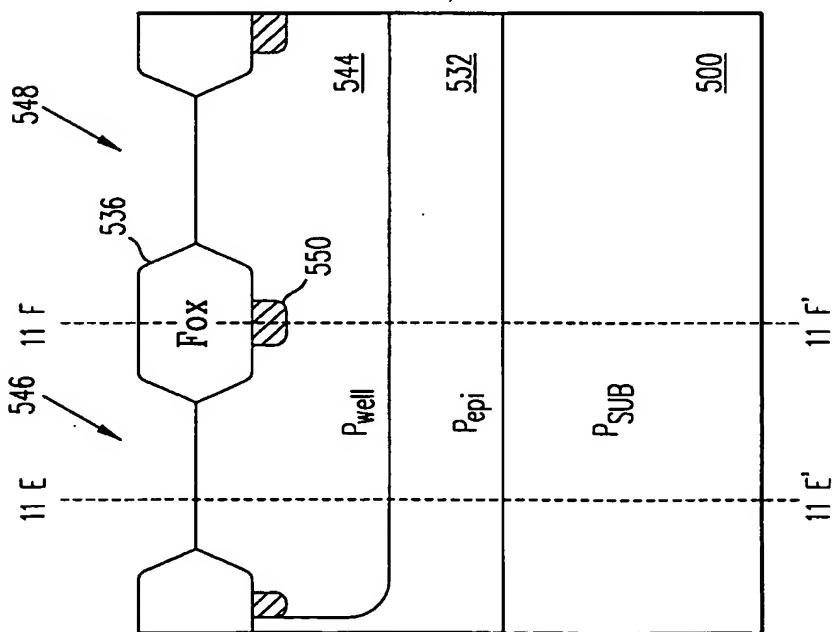


FIG. 11G

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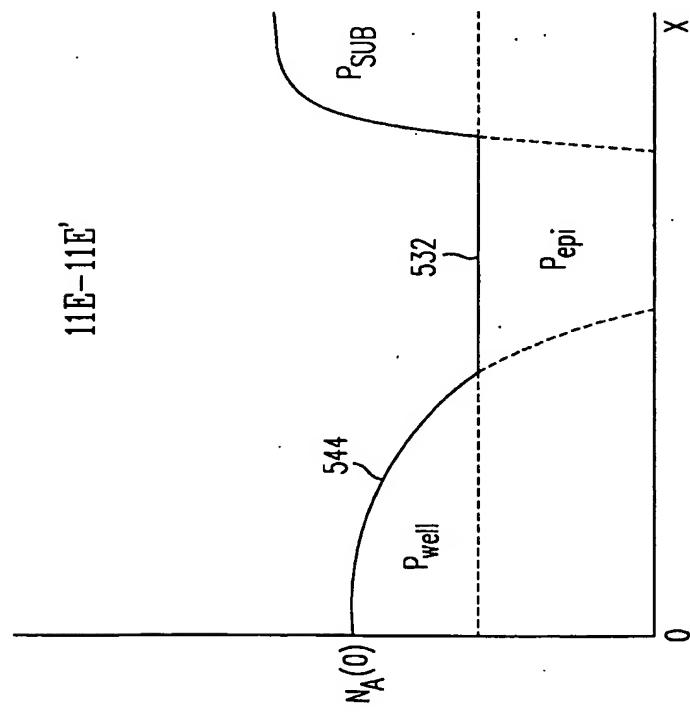
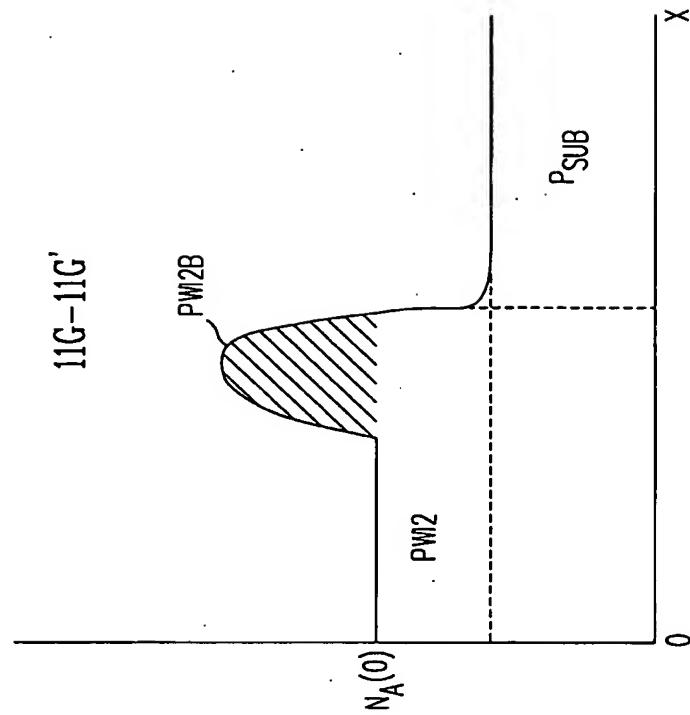


FIG. 11J

FIG. 11I

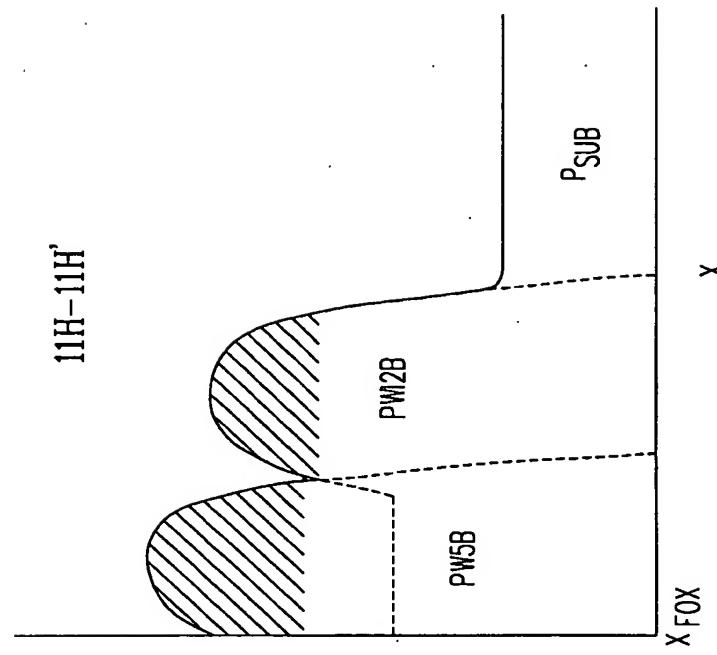


FIG. 11L

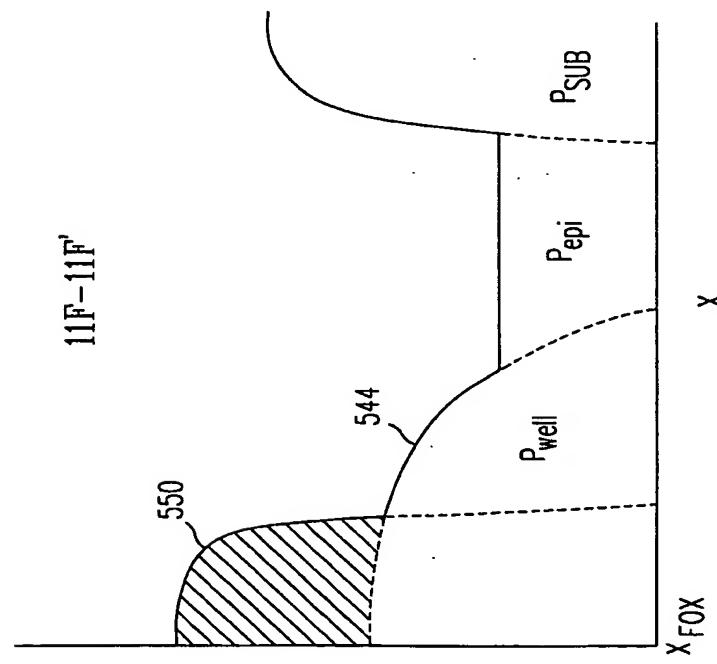


FIG. 11K

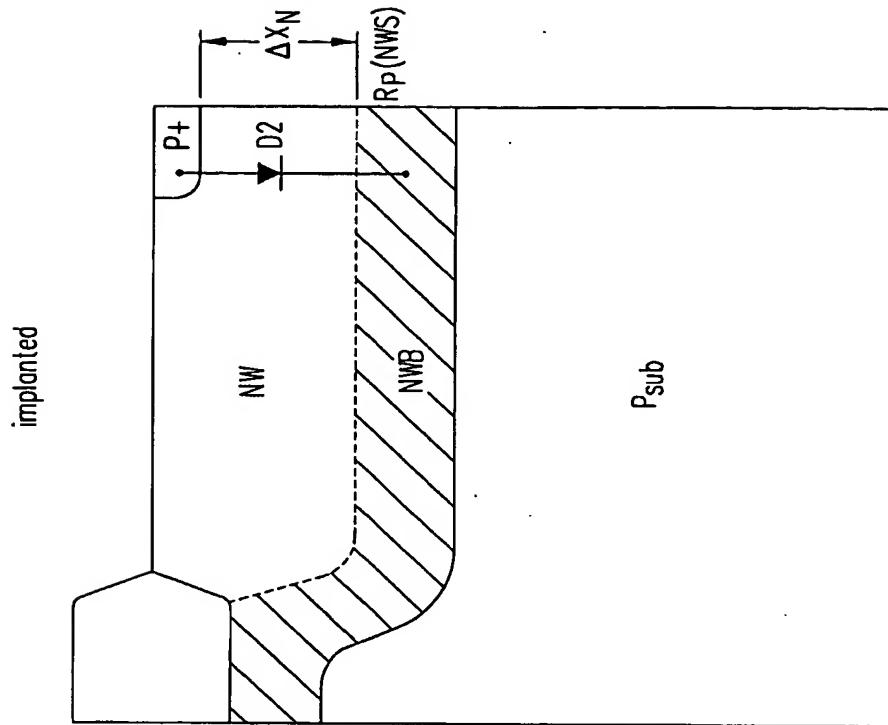


FIG. 12B

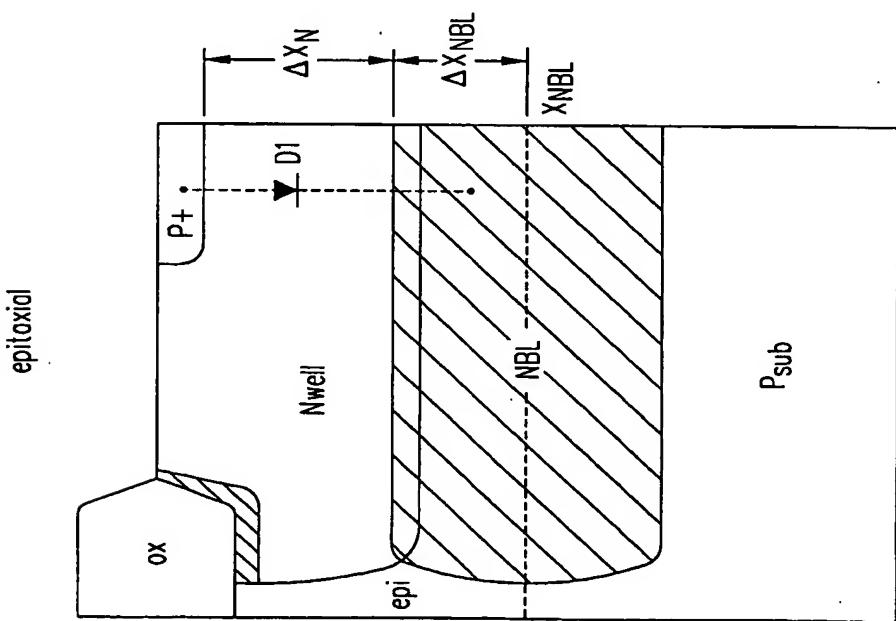


FIG. 12A

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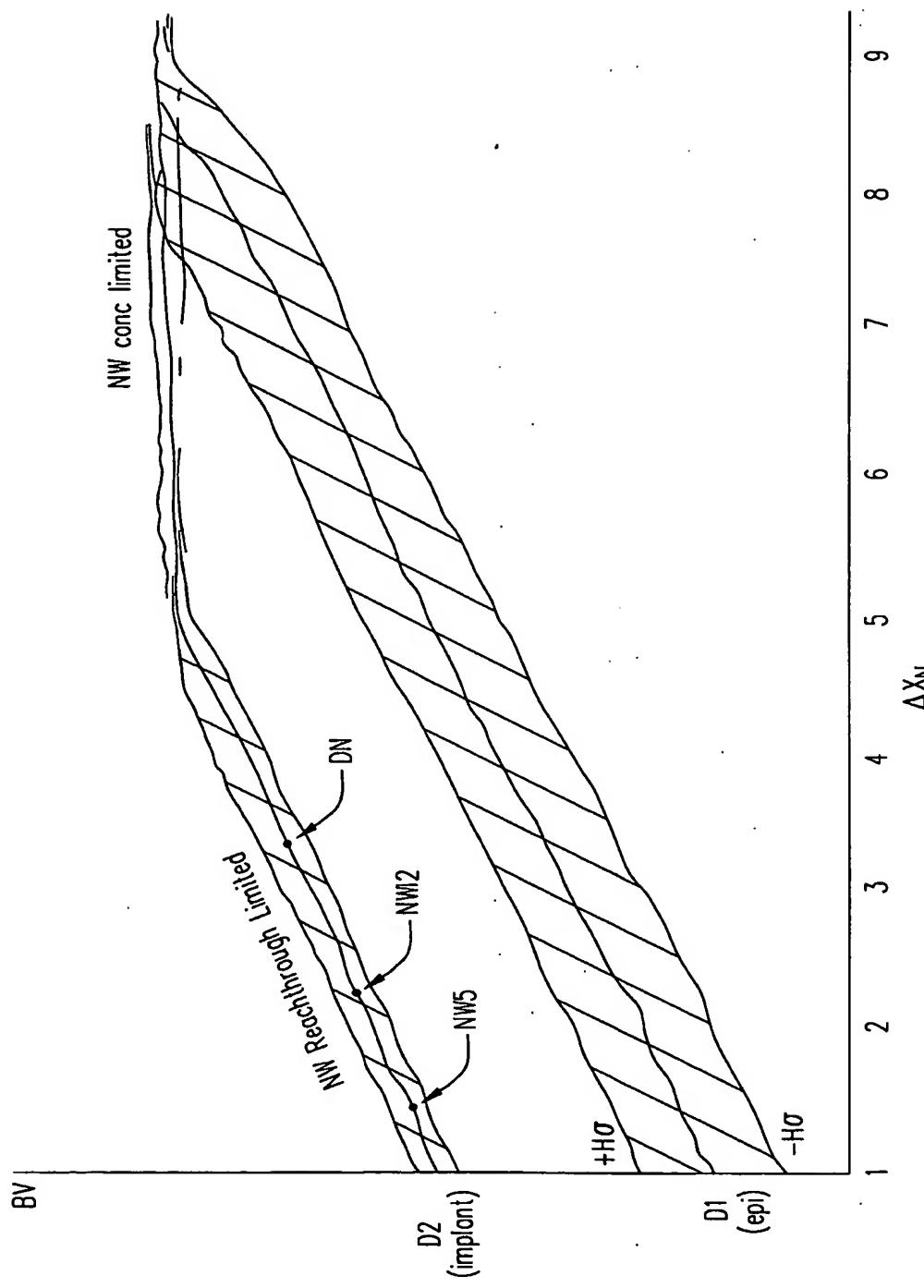


FIG. 12C

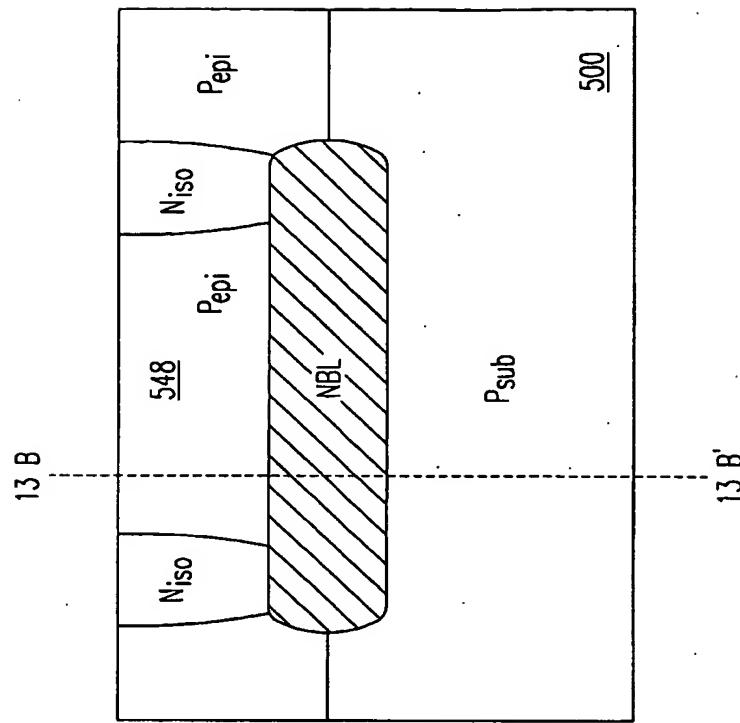


FIG. 13B
(Prior Art)

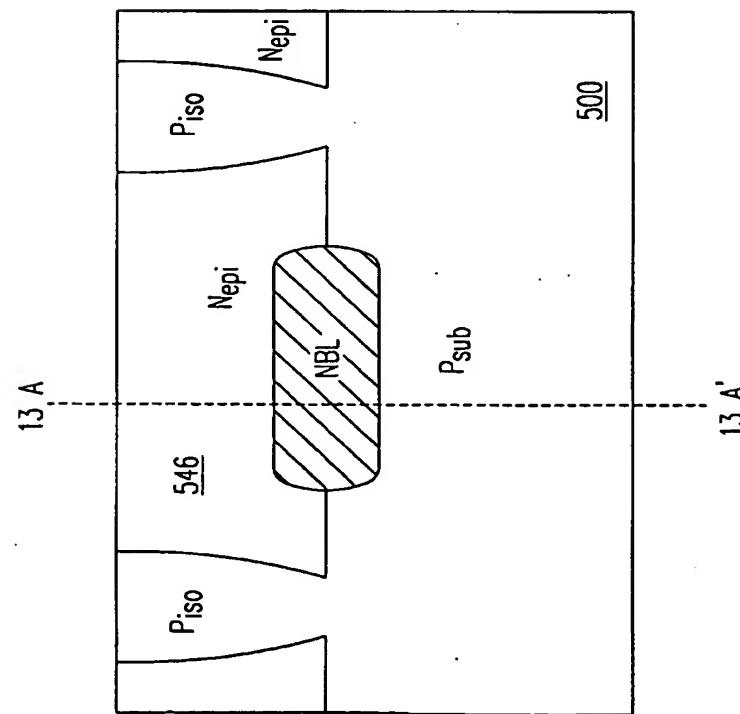
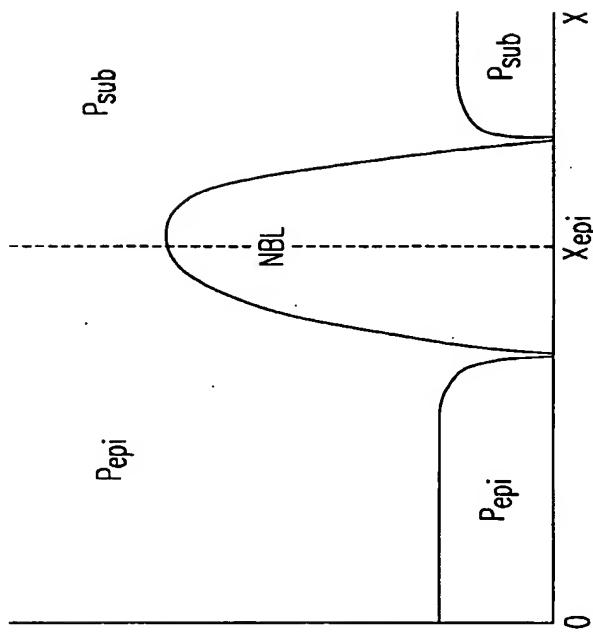


FIG. 13A
(Prior Art)

13B-13B'



13A-13A'

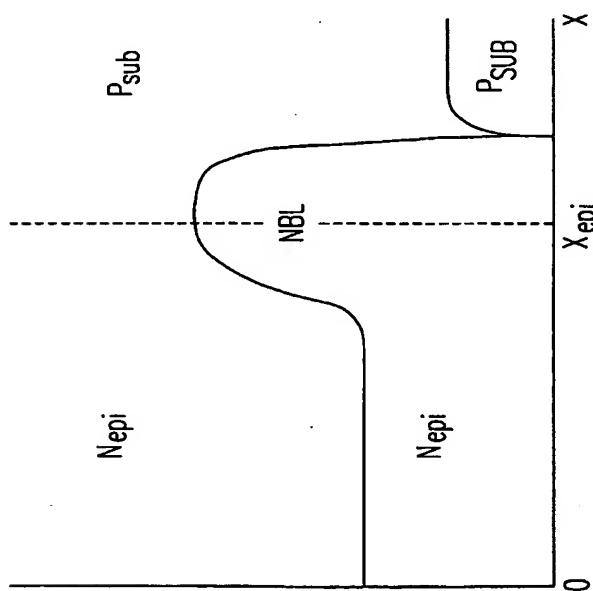


FIG. 13C

FIG. 13D

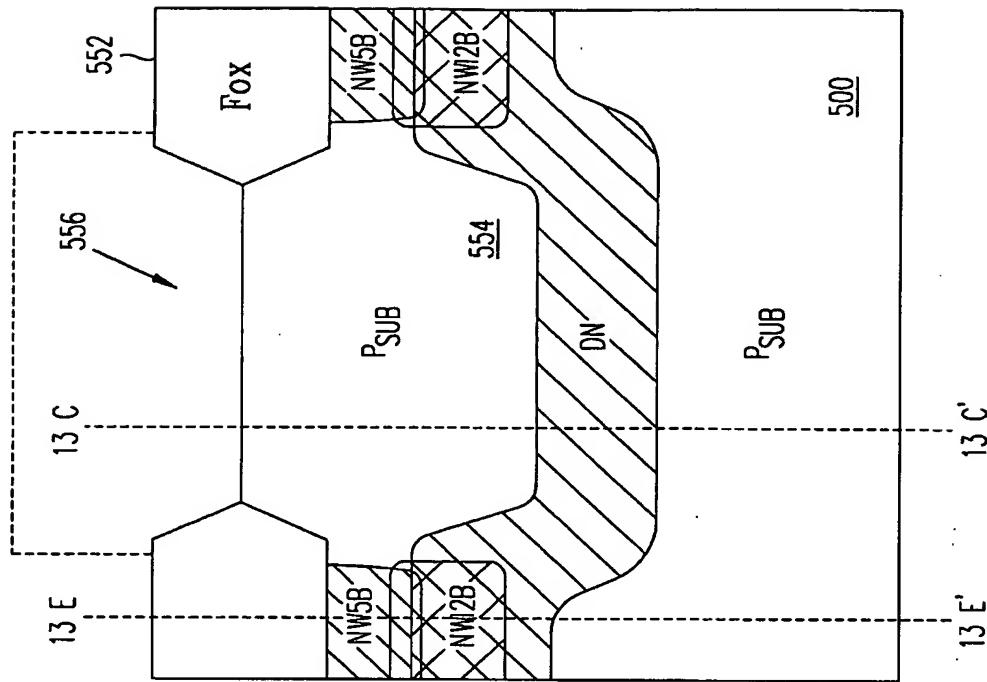


FIG. 13F

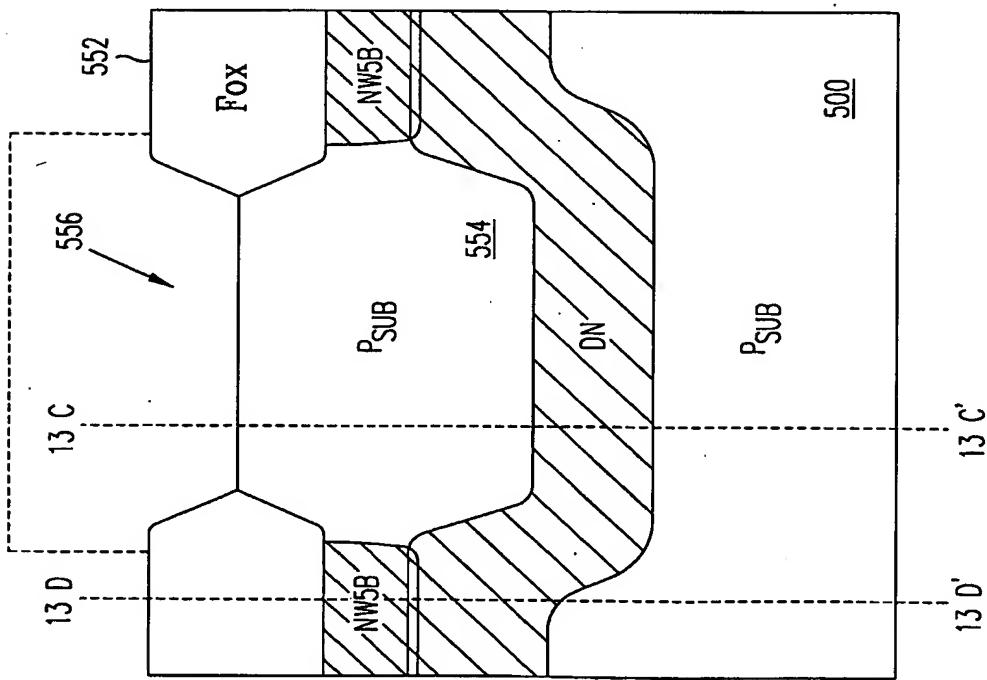
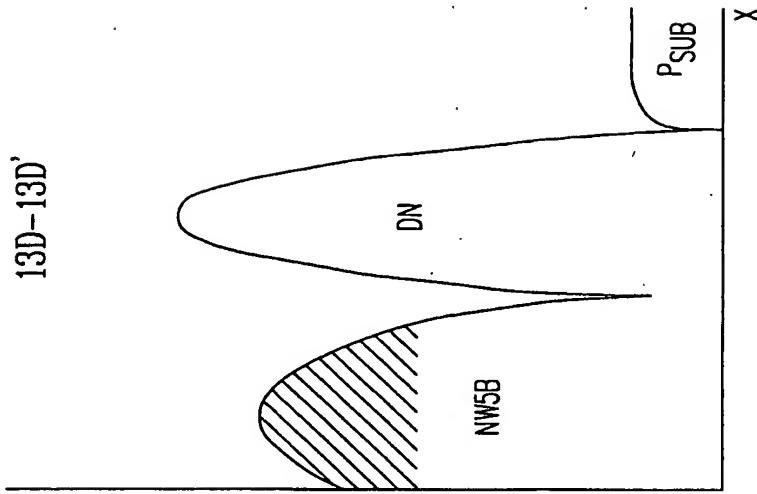


FIG. 13E

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13D-13D'



13C-13C'

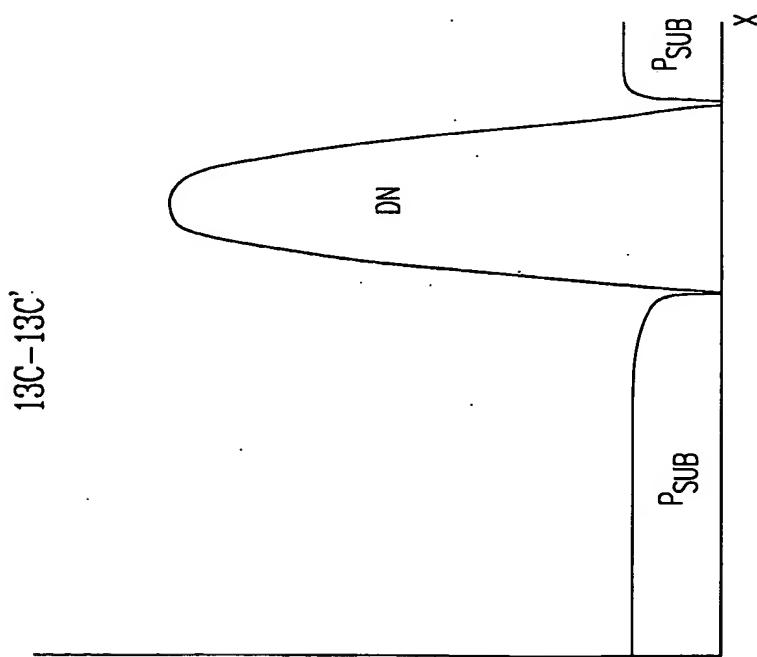


FIG. 13H

FIG. 13G

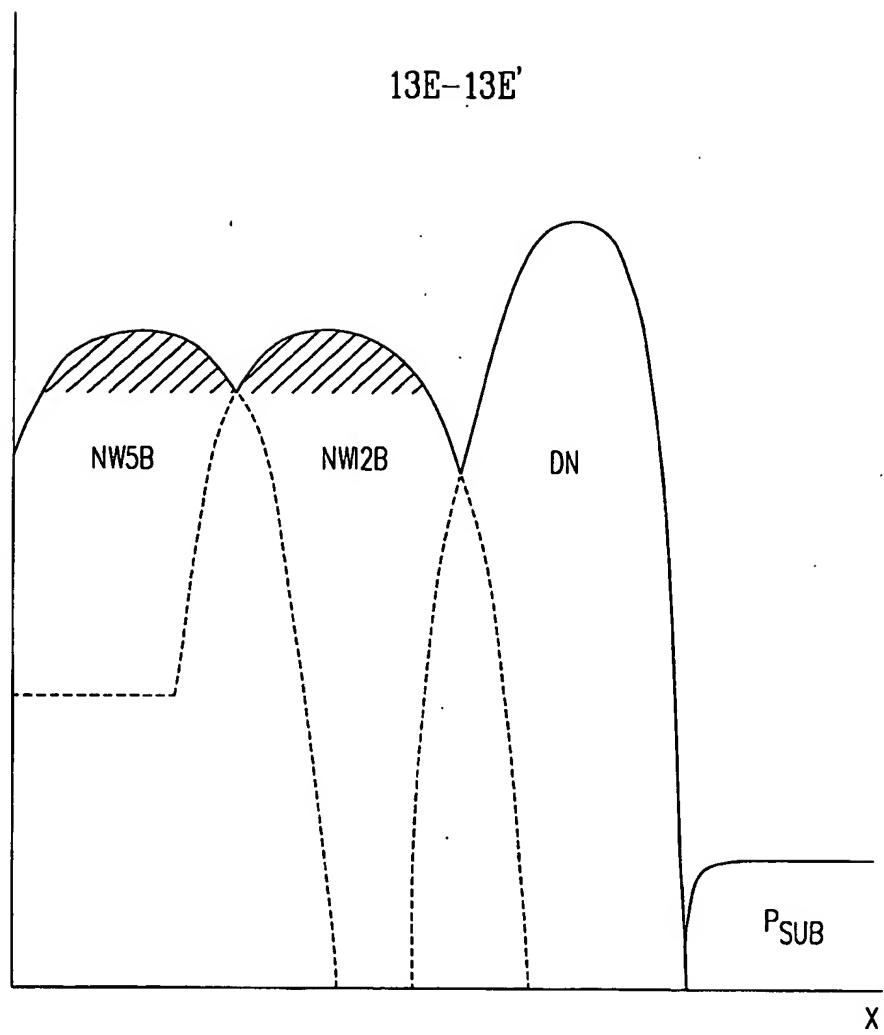


FIG. 13I

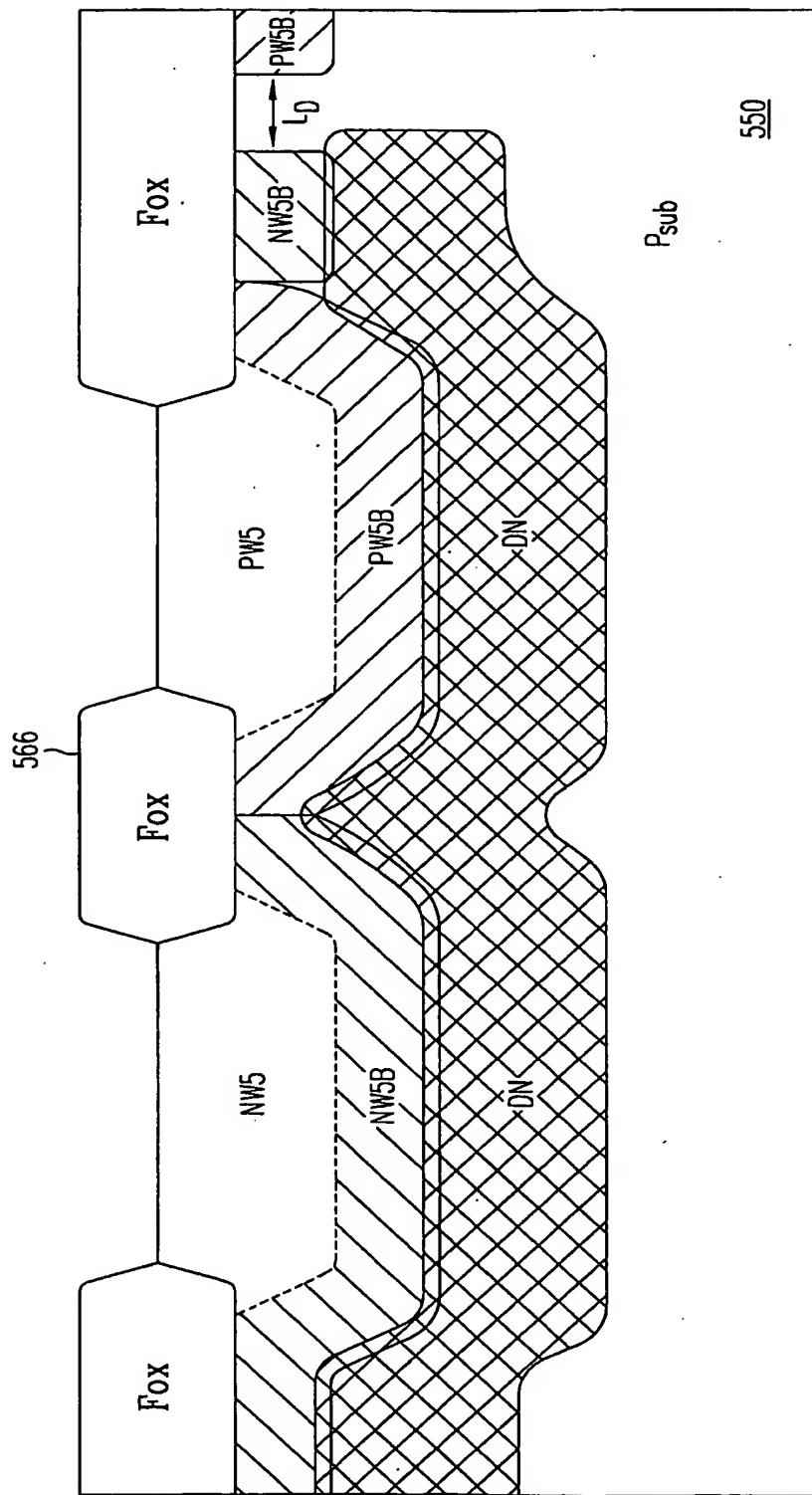


FIG. 14A

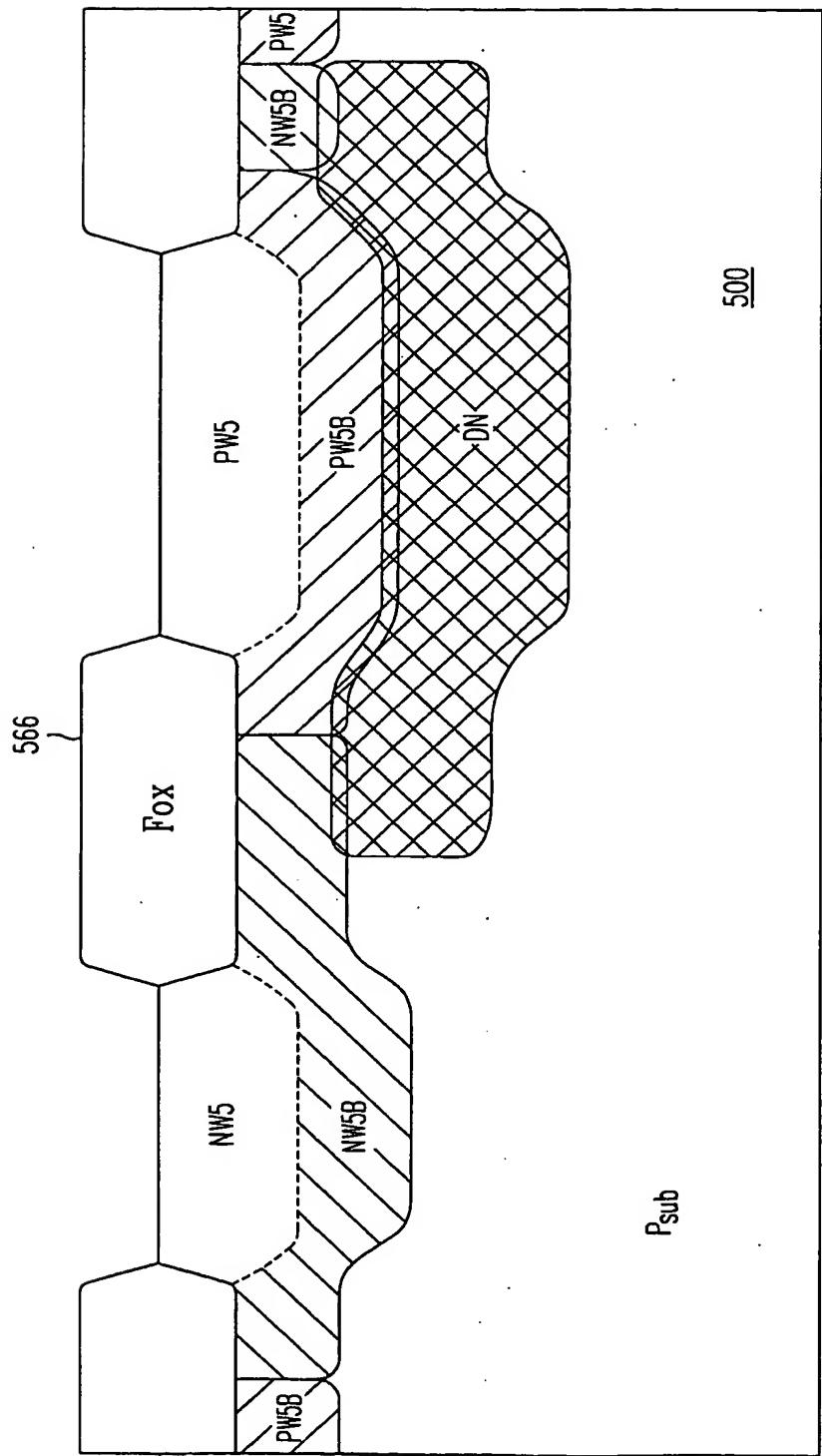


FIG. 14B

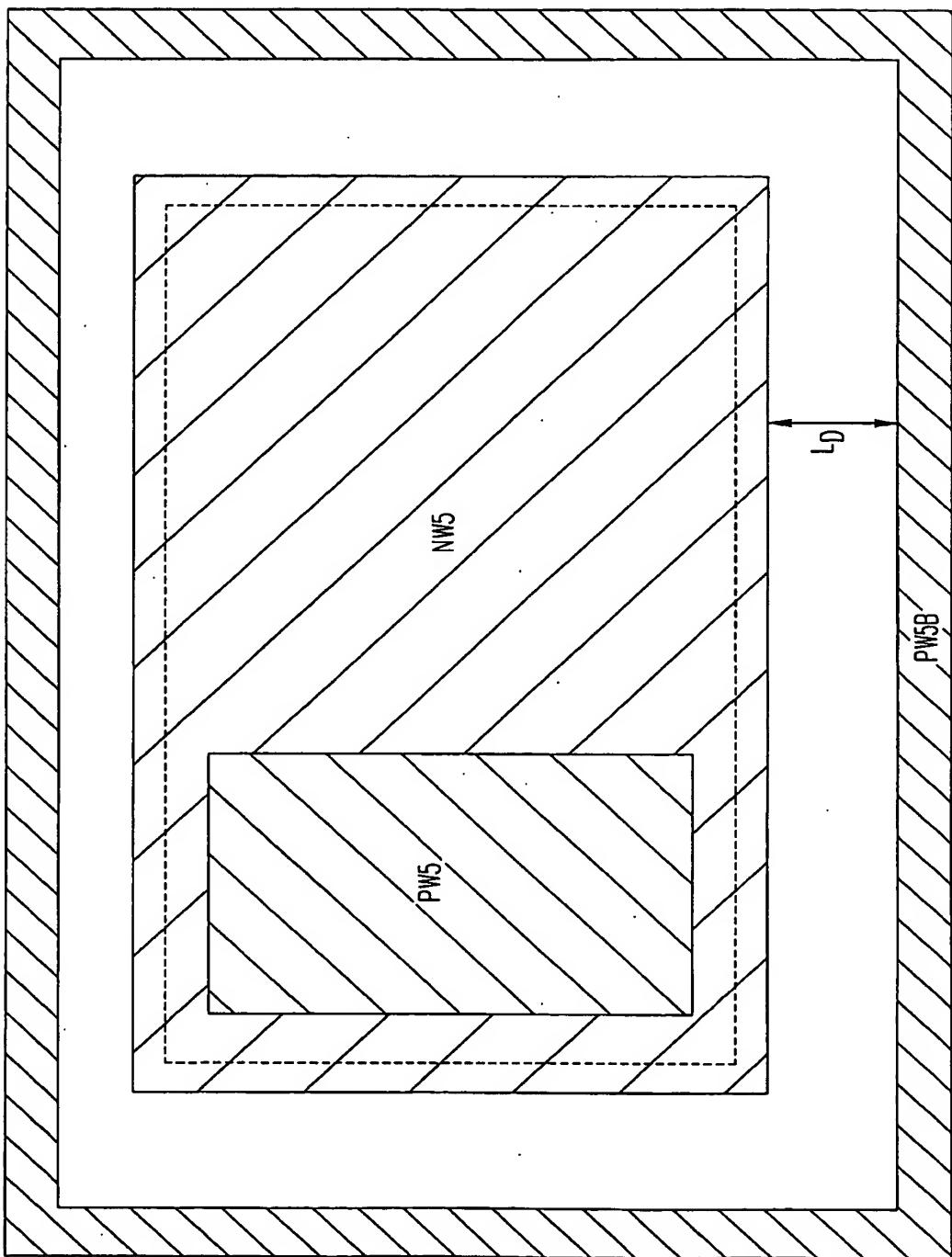


FIG. 14C

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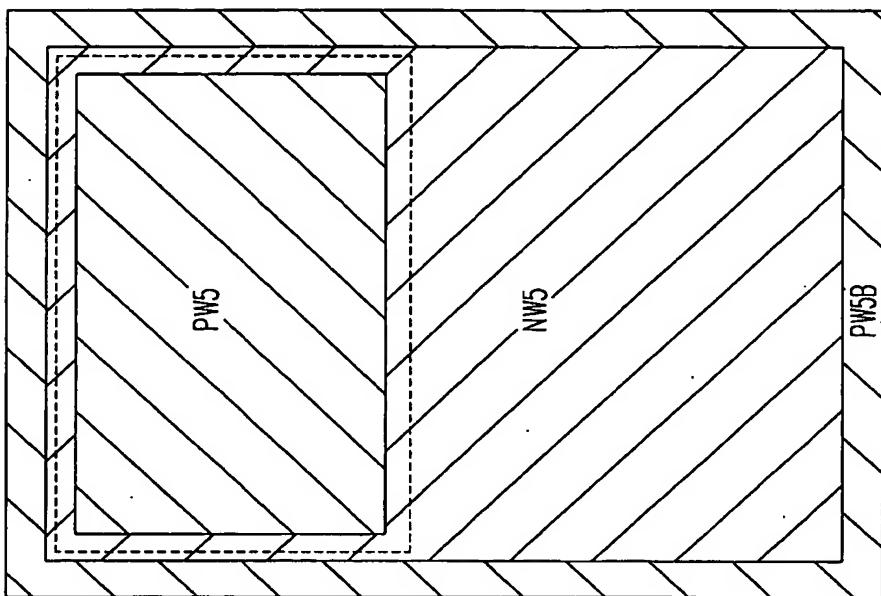


FIG. 14E

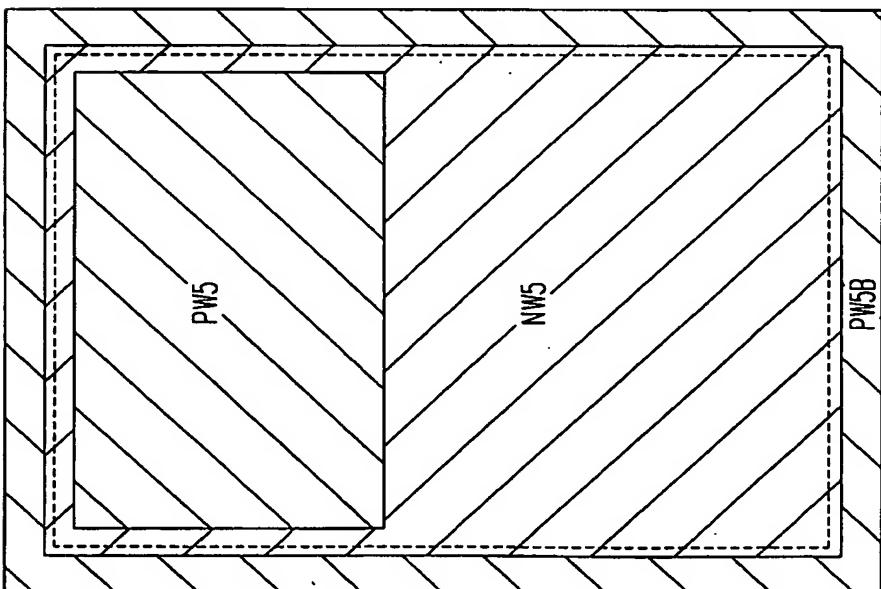


FIG. 14D

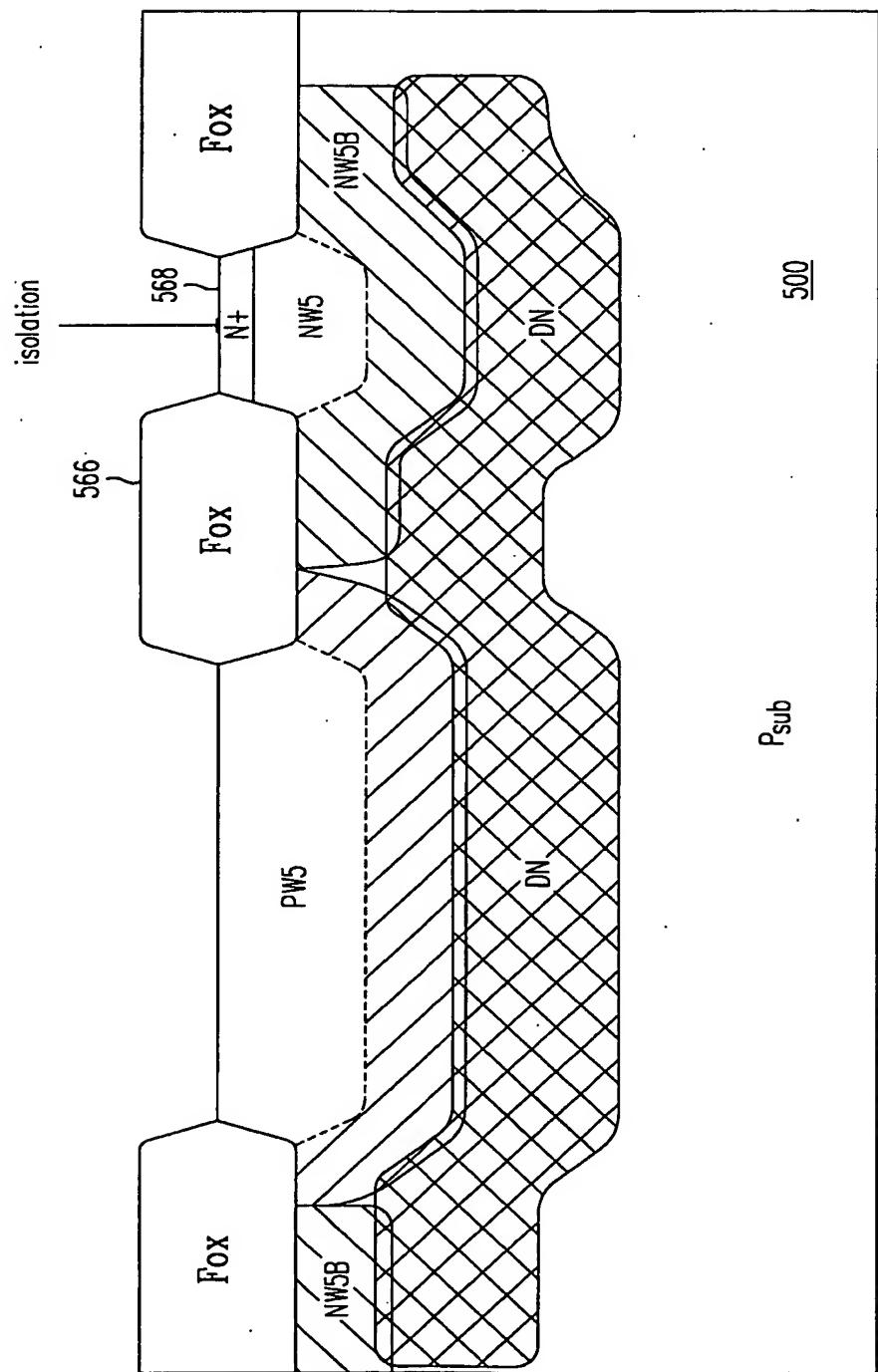


FIG. 14F

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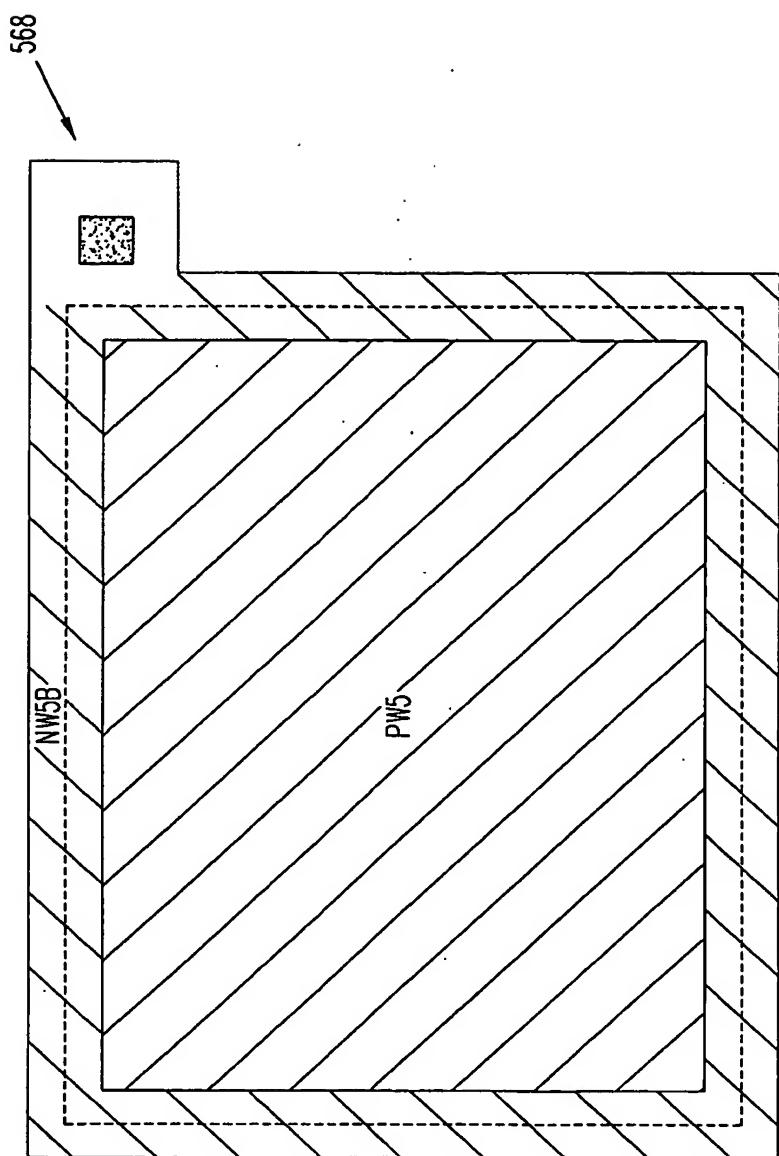


FIG. 14C

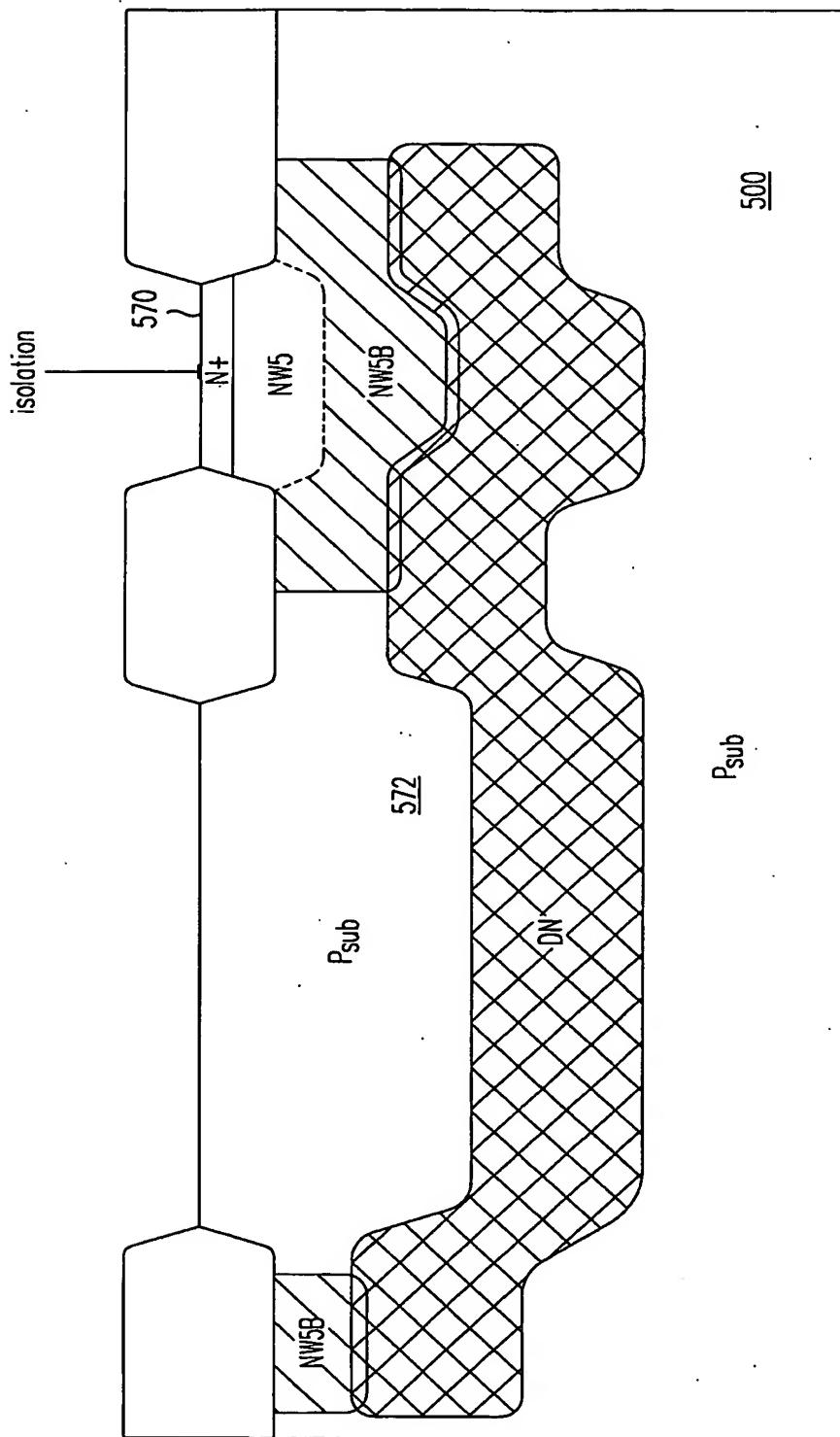


FIG. 14H

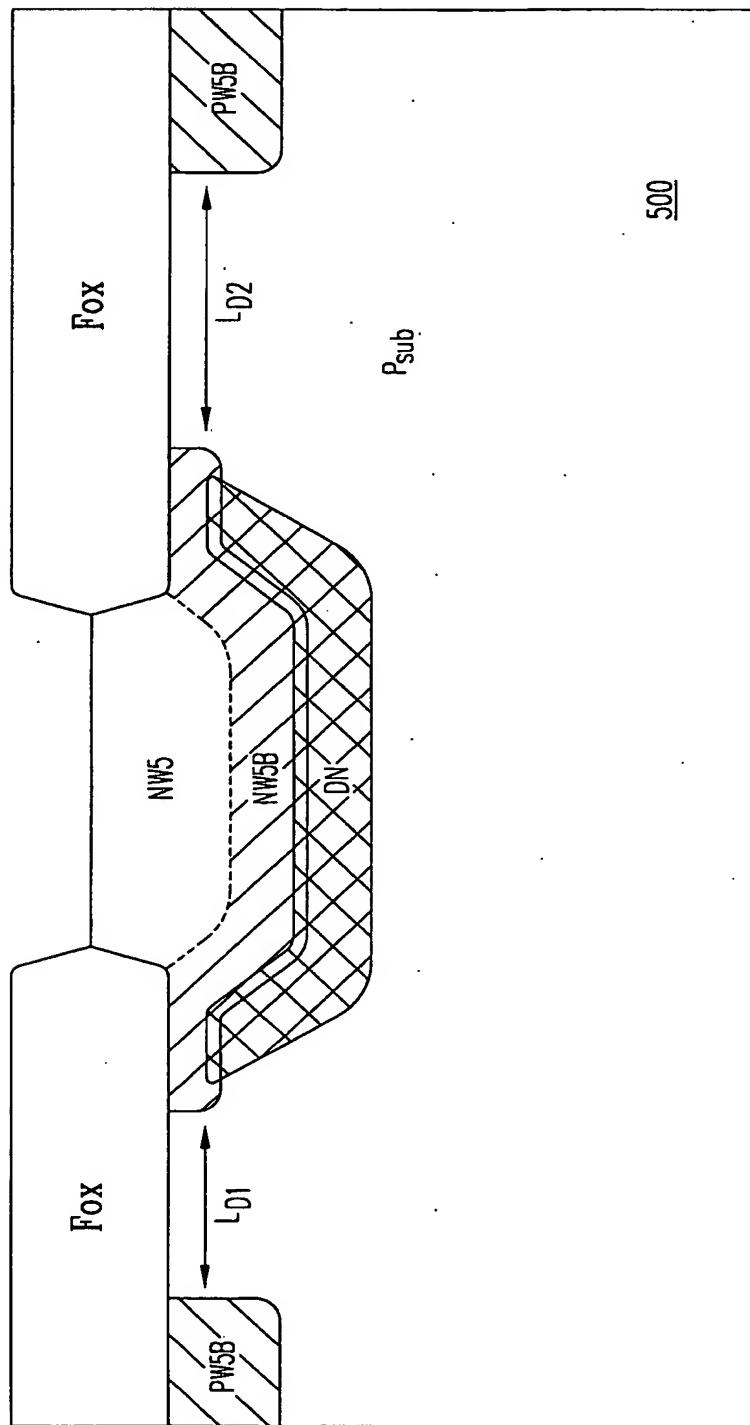


FIG. 141

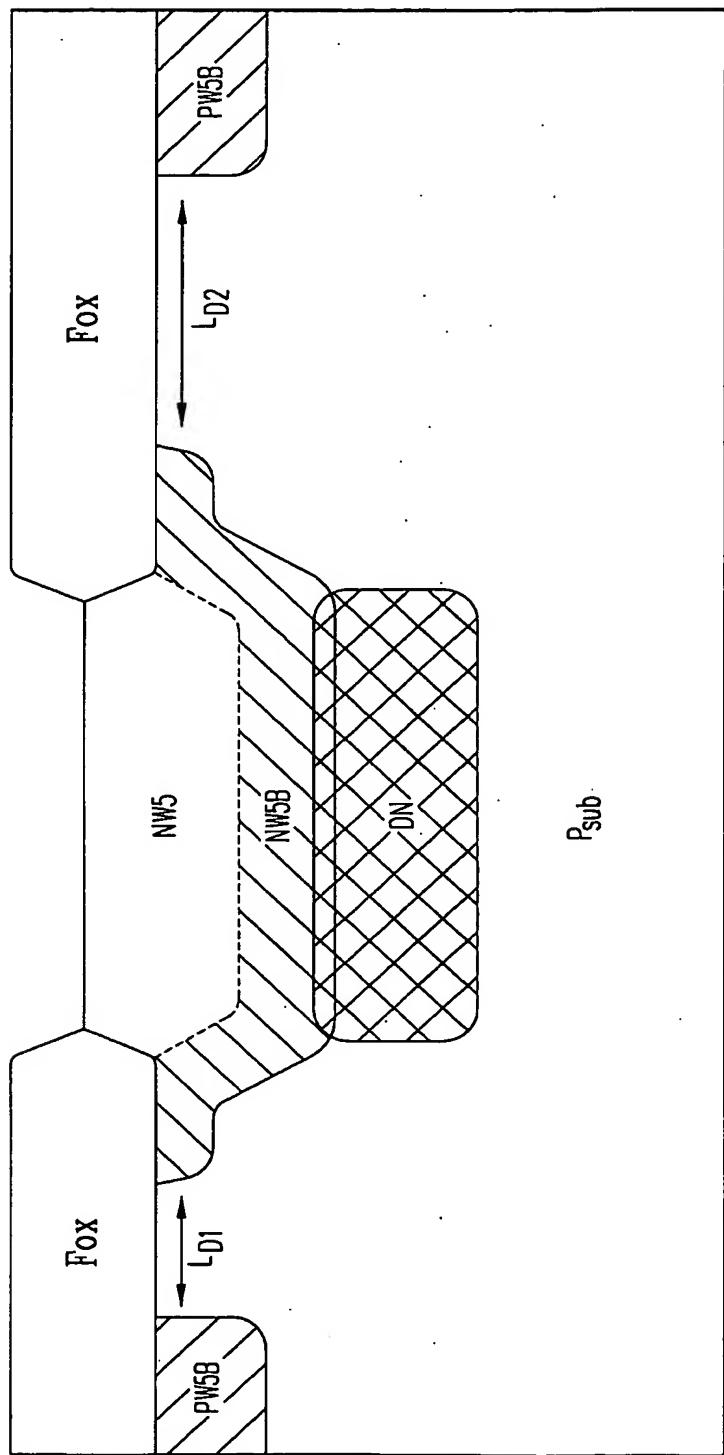
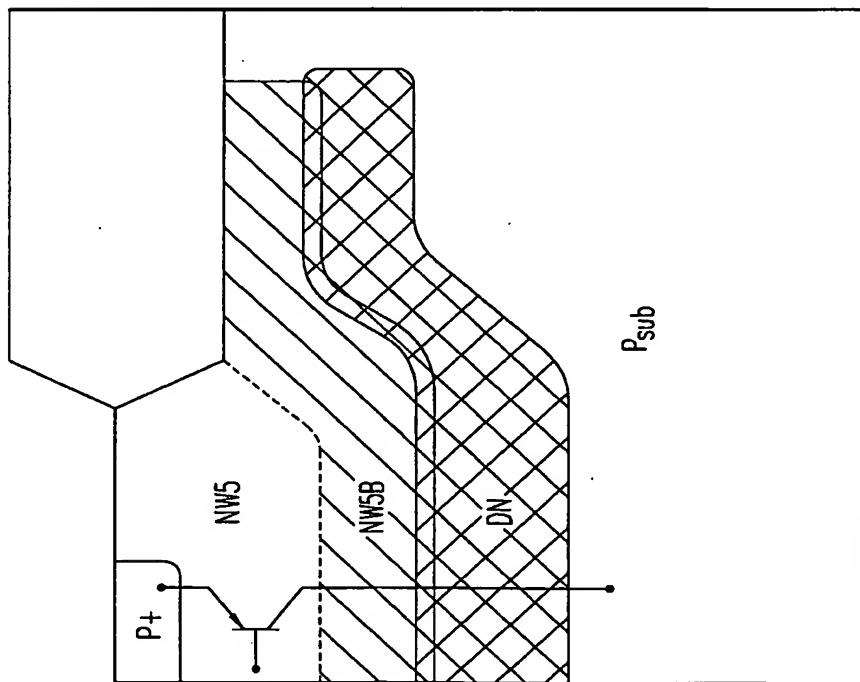
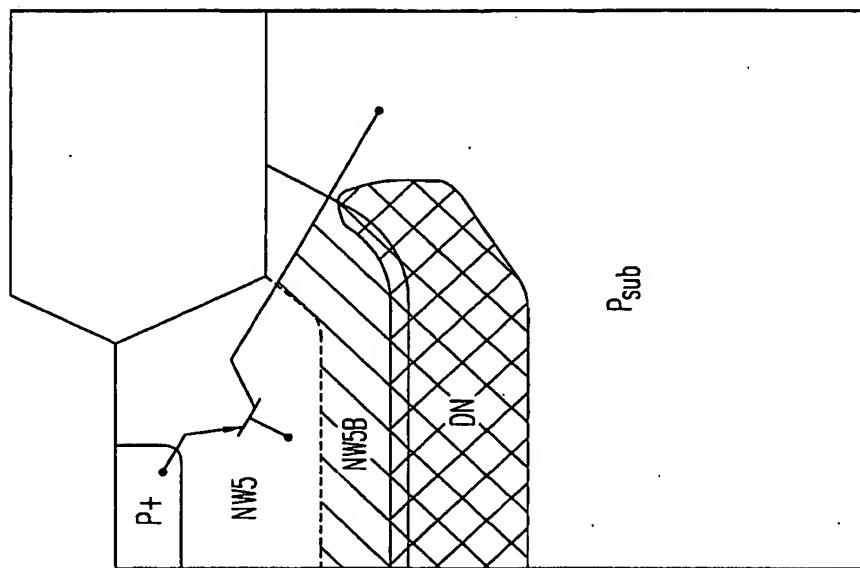


FIG. 14J



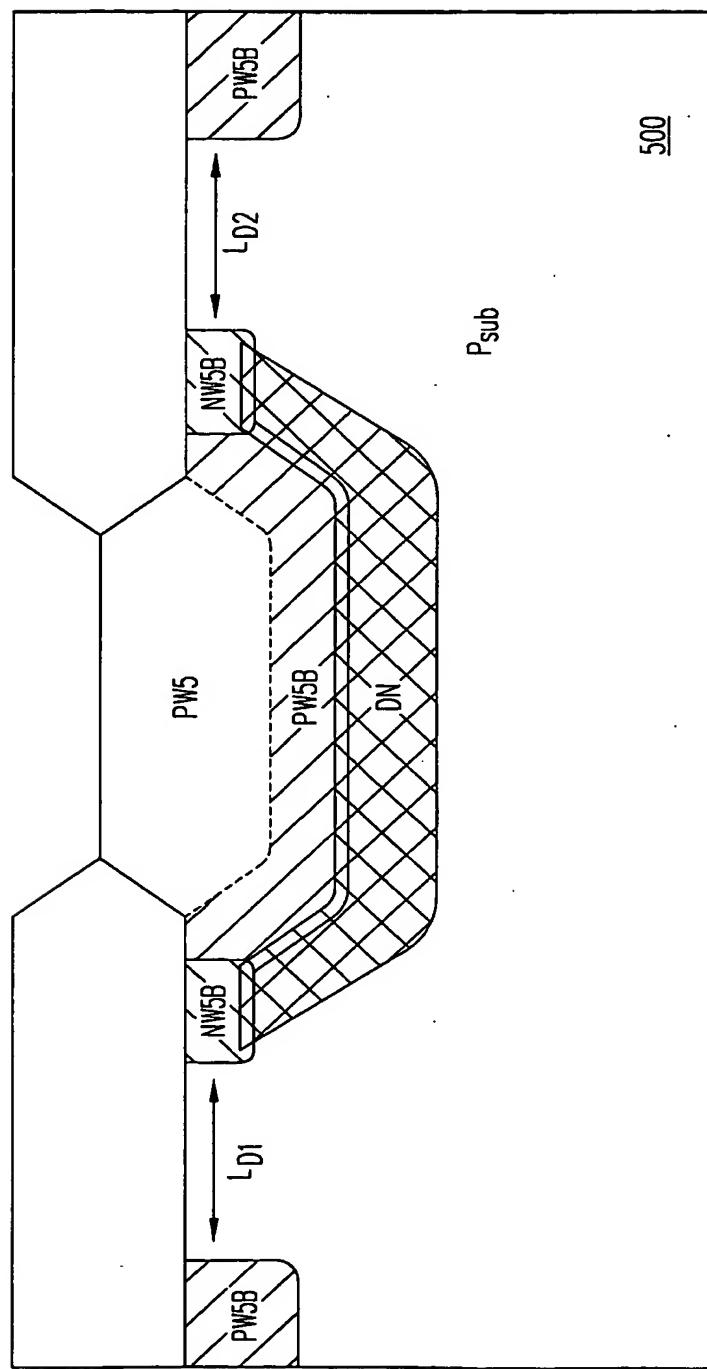
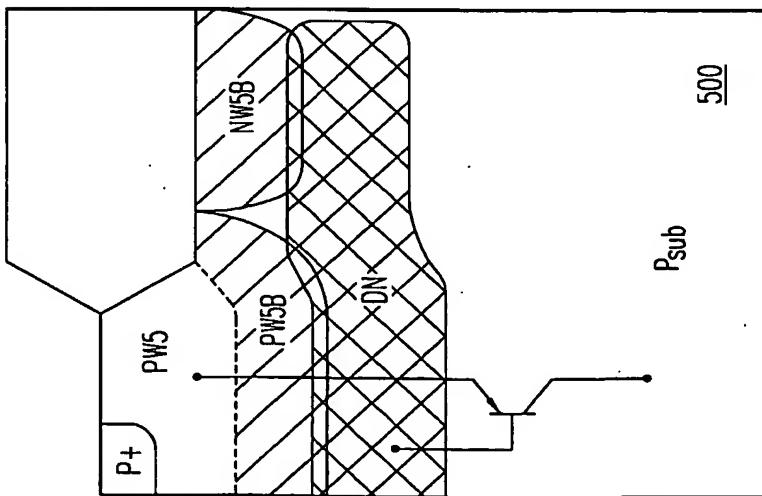
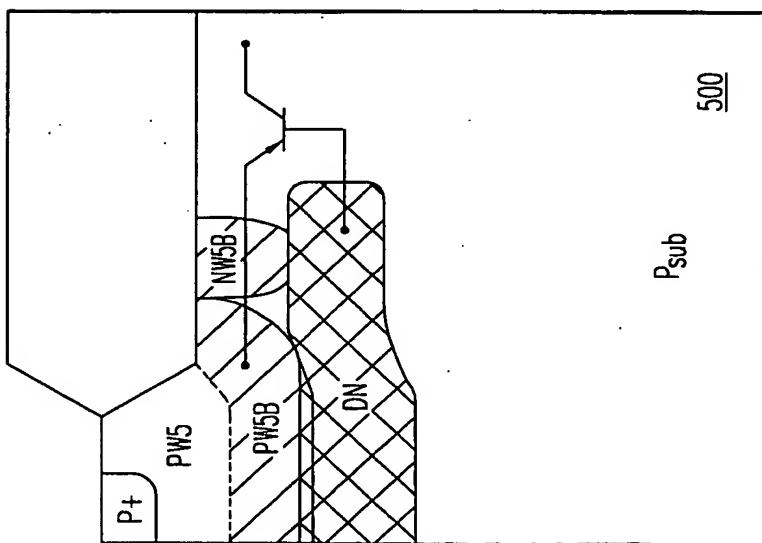
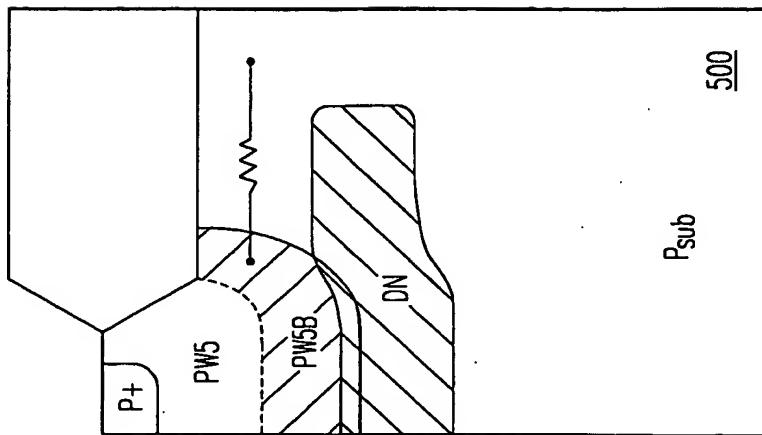


FIG. 14M



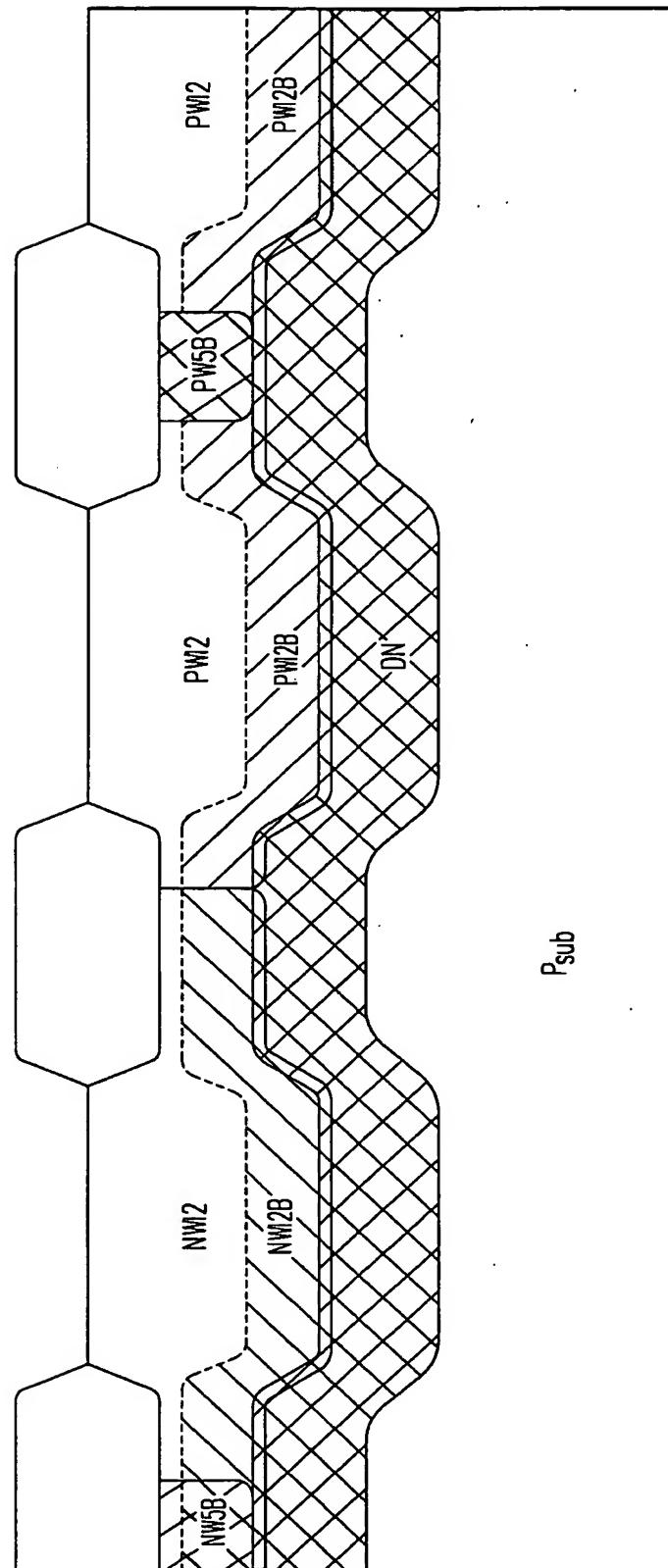


FIG. 15A

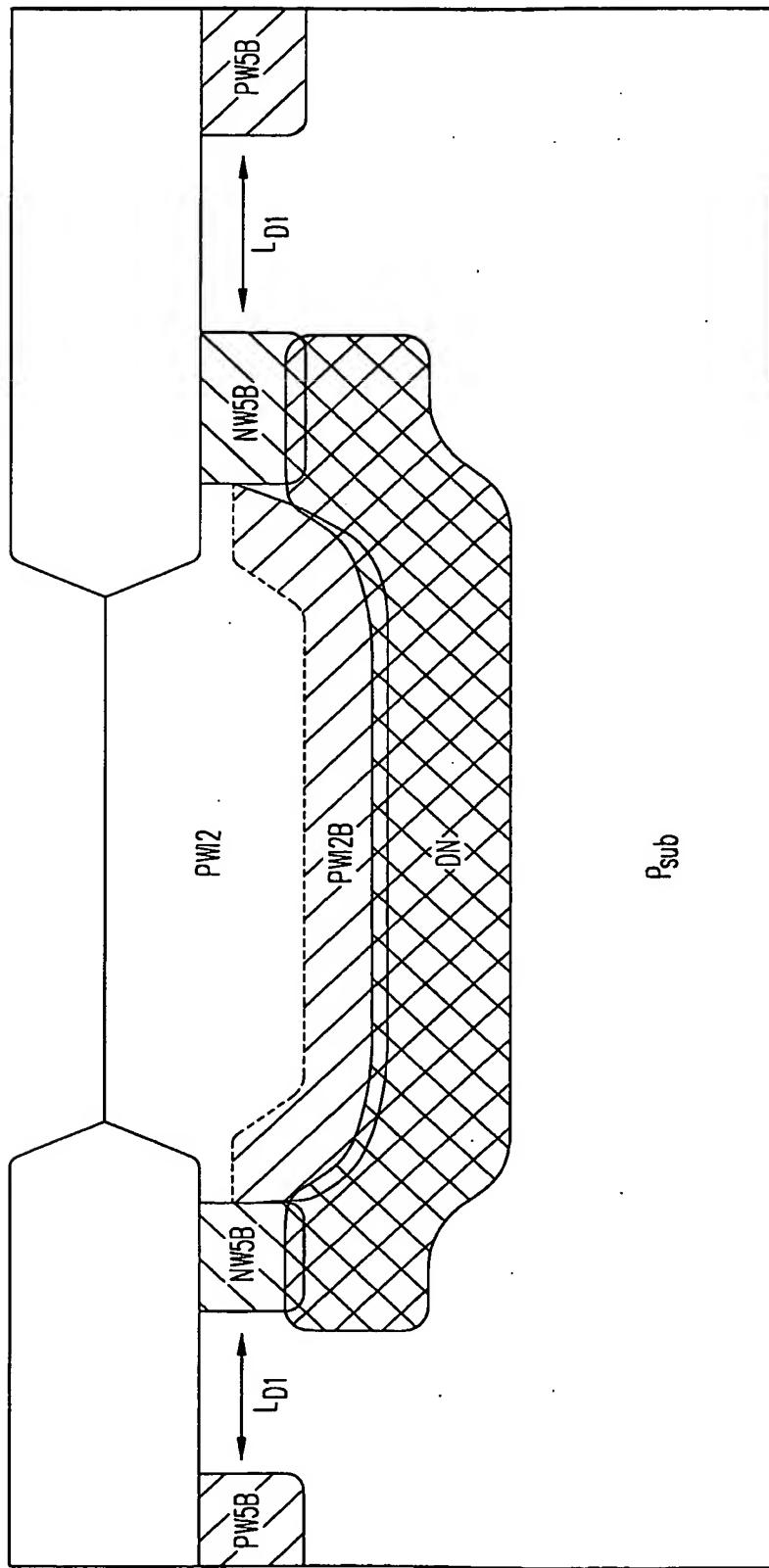


FIG. 15B

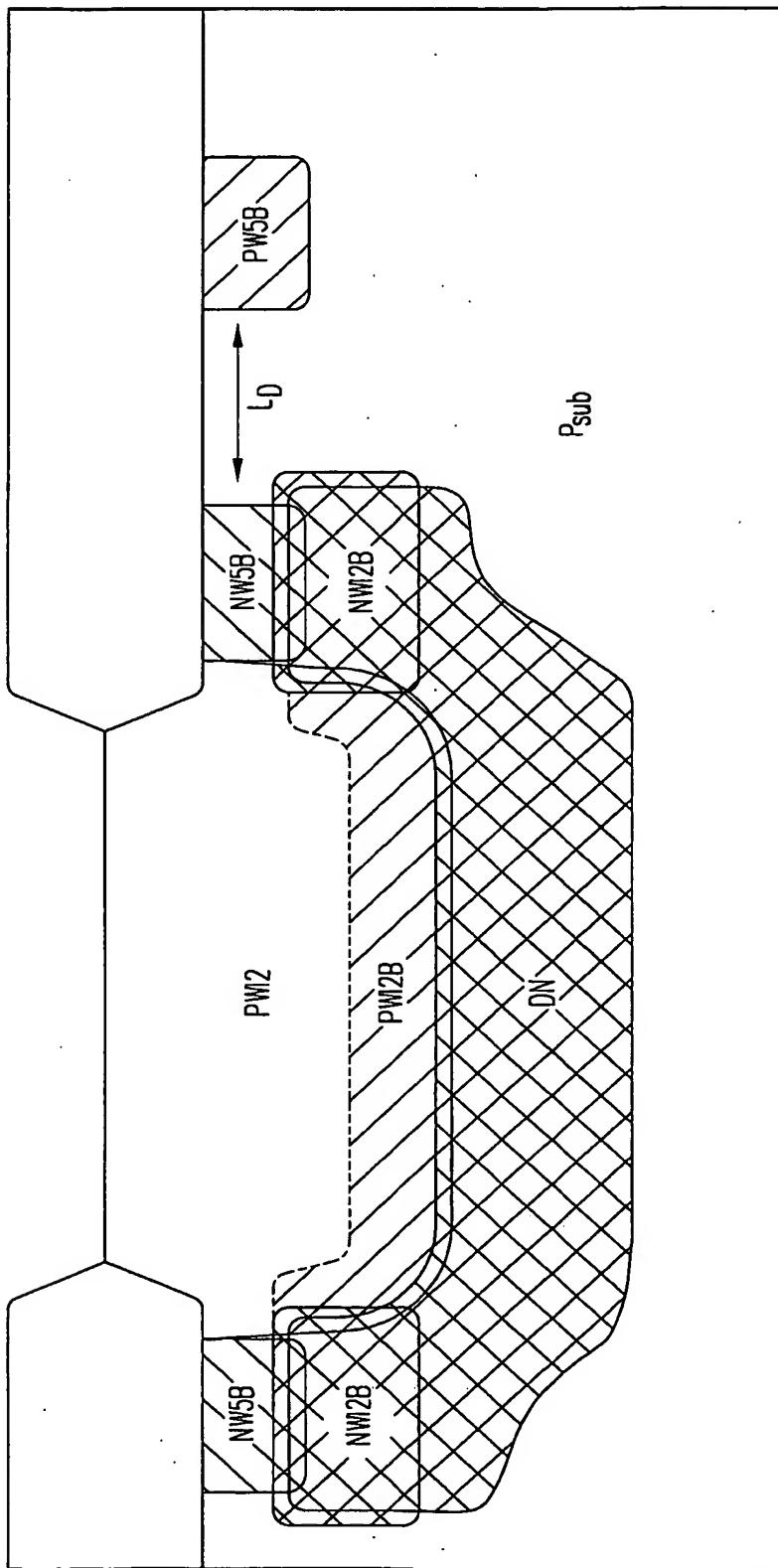


FIG. 15C

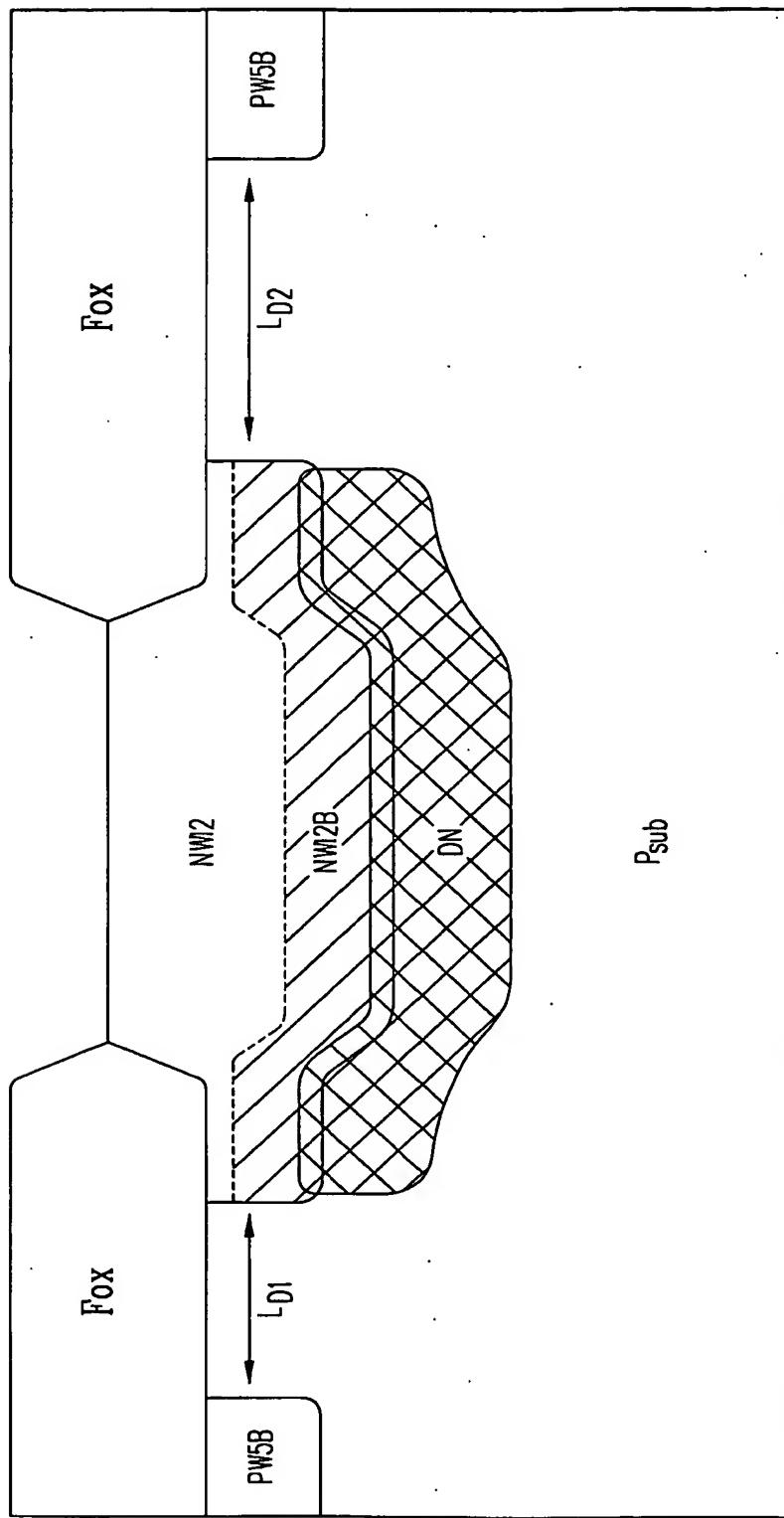
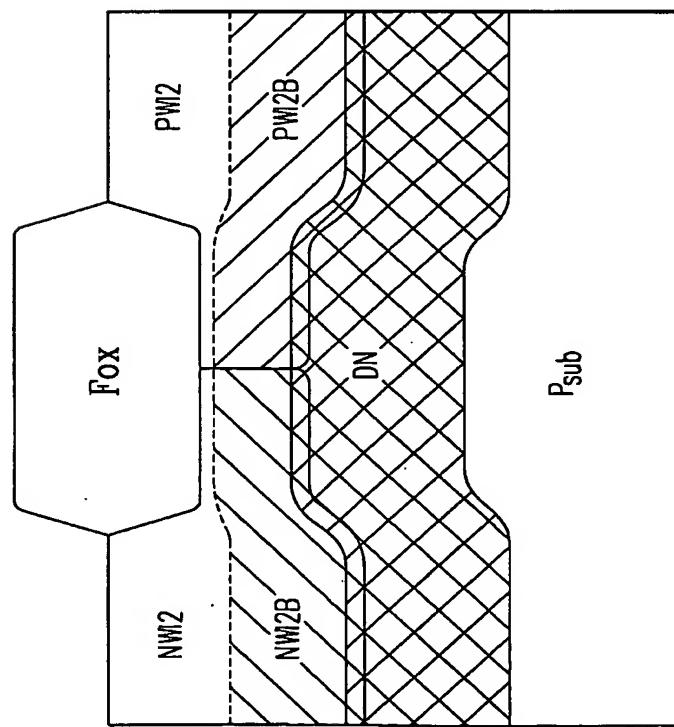
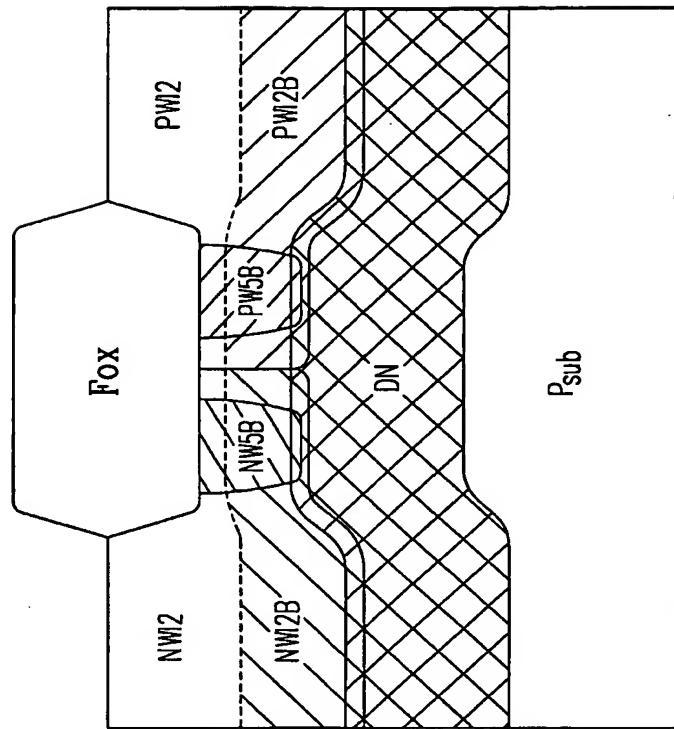


FIG. 15D



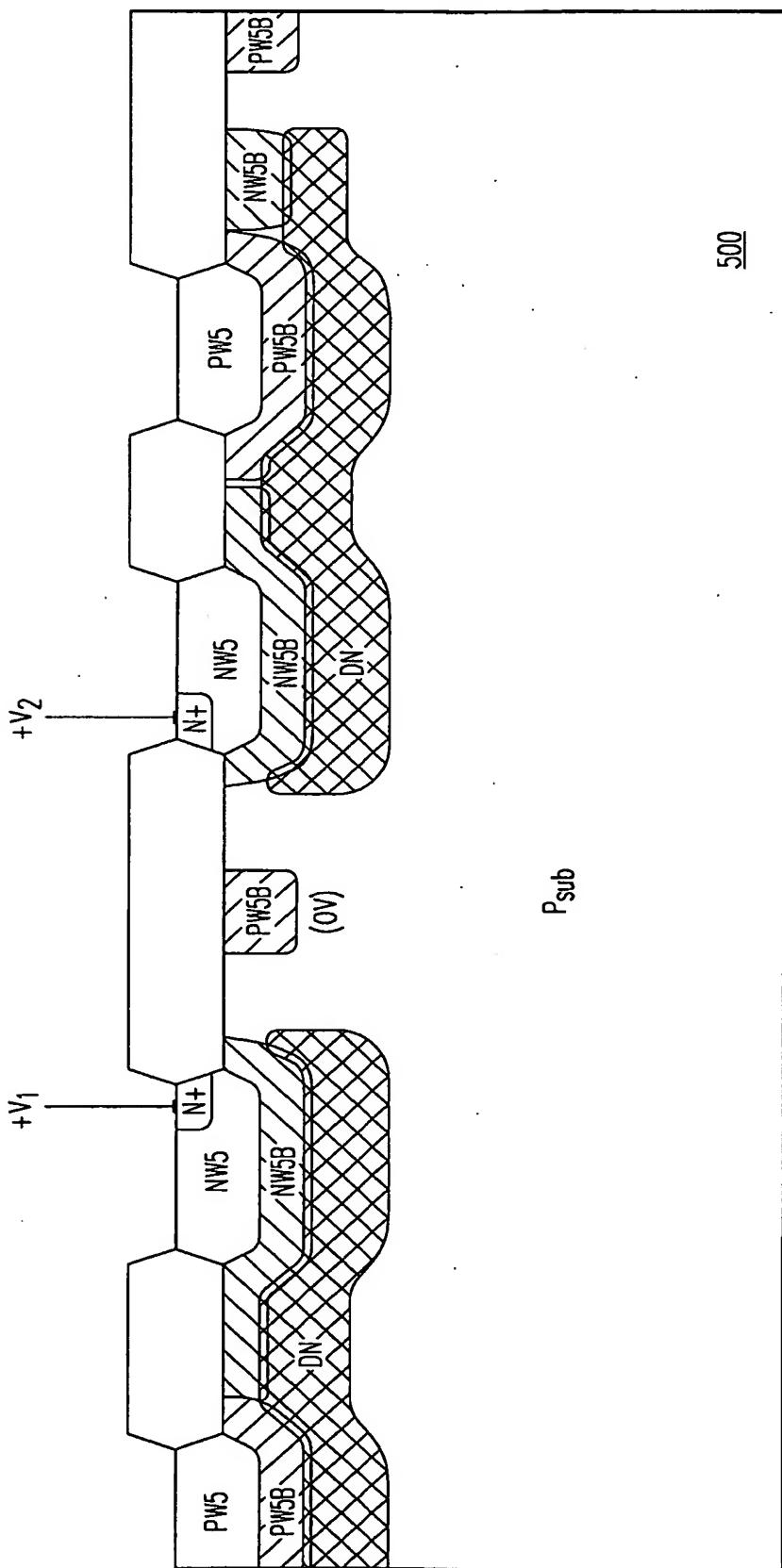
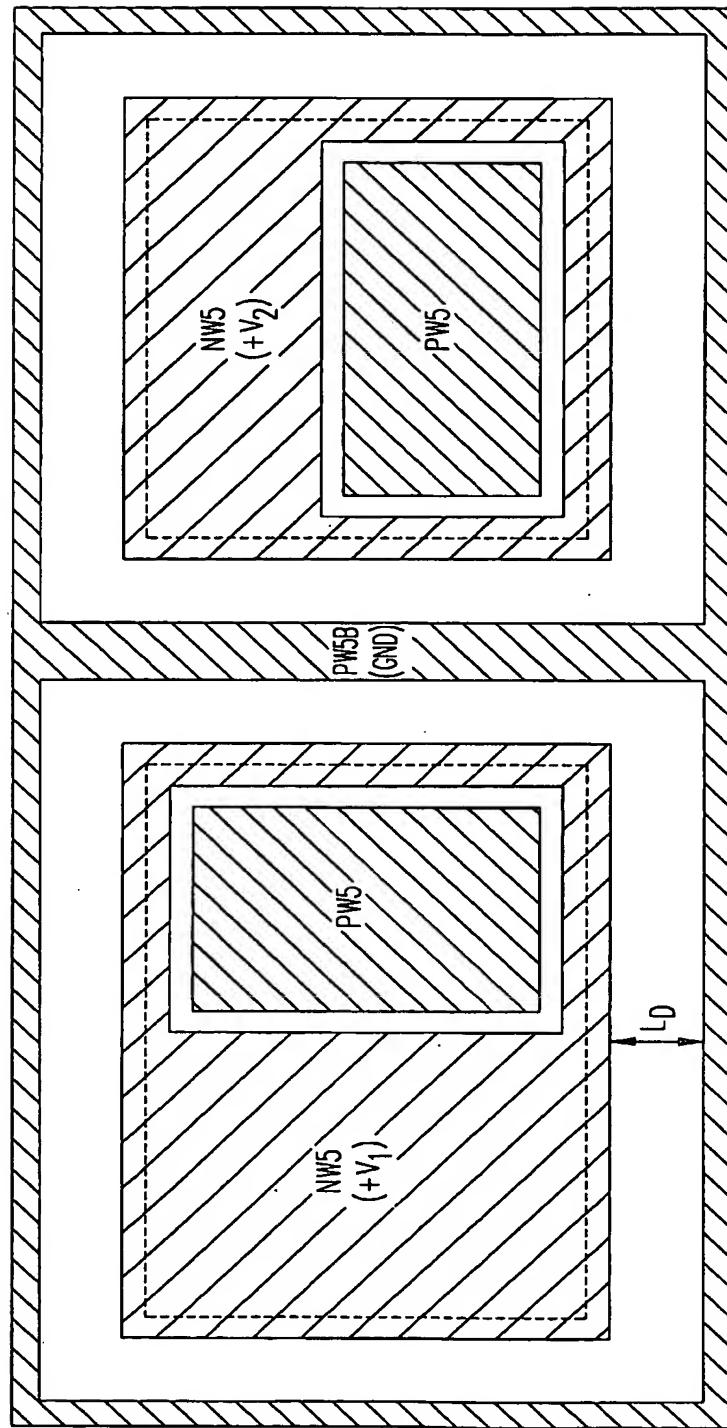


FIG. 16A



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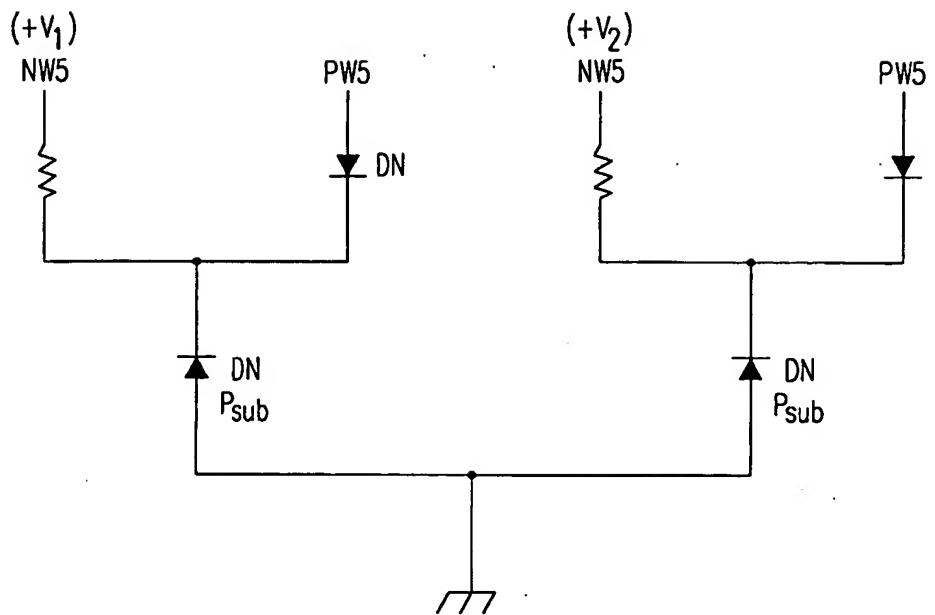


FIG. 16C

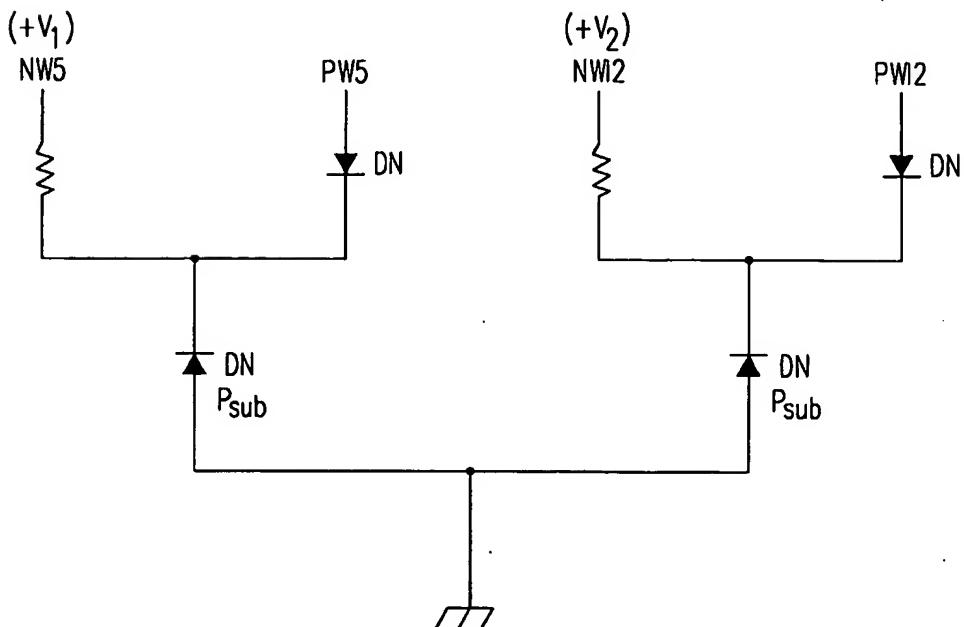


FIG. 16E

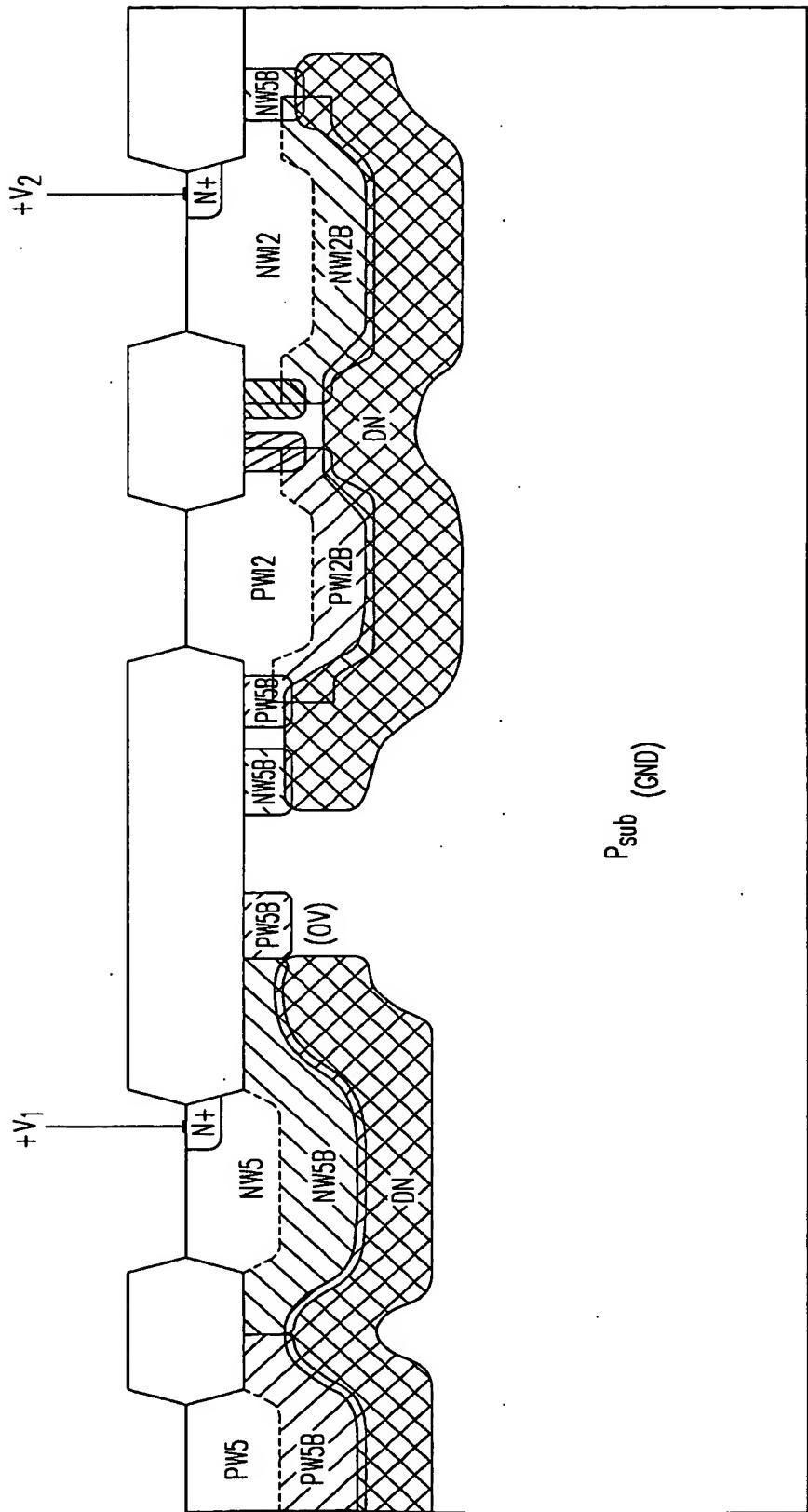


FIG. 16D

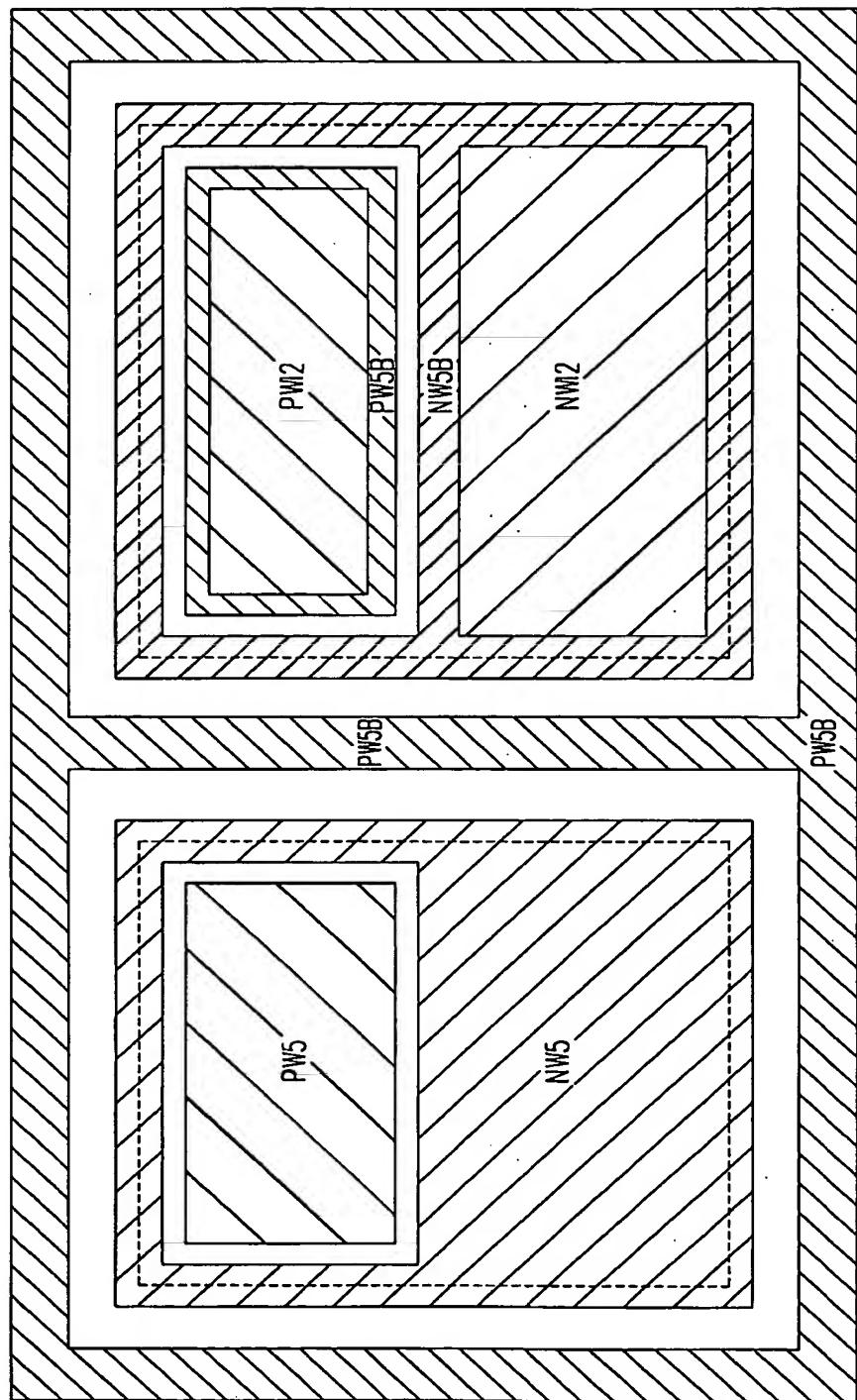


FIG. 16F

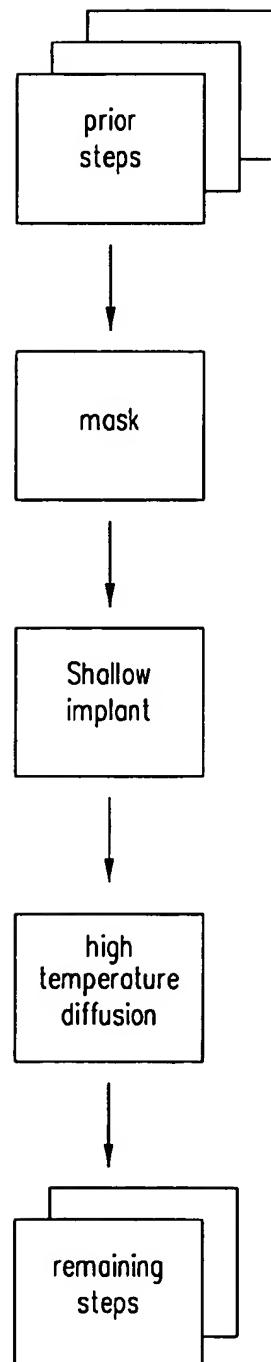


FIG. 17A
(Prior Art)

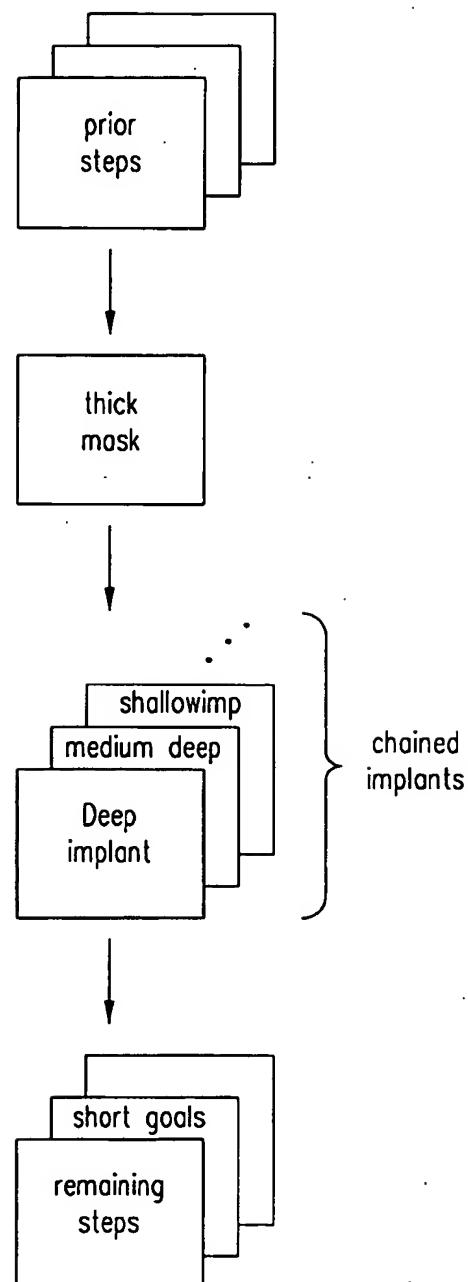


FIG. 17B

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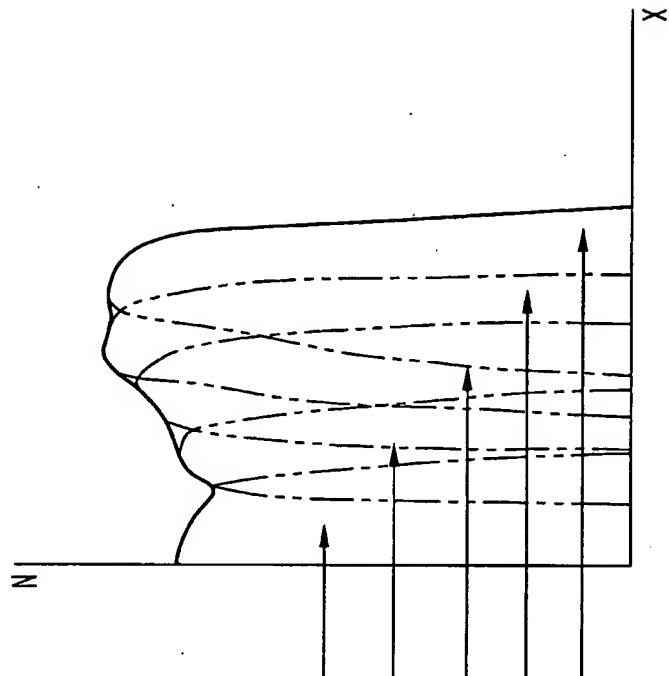


FIG. 17D

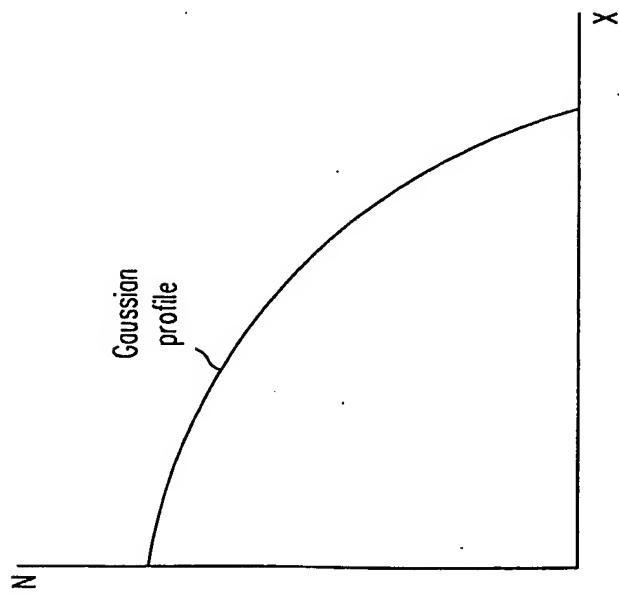


FIG. 17C
(Prior Att)

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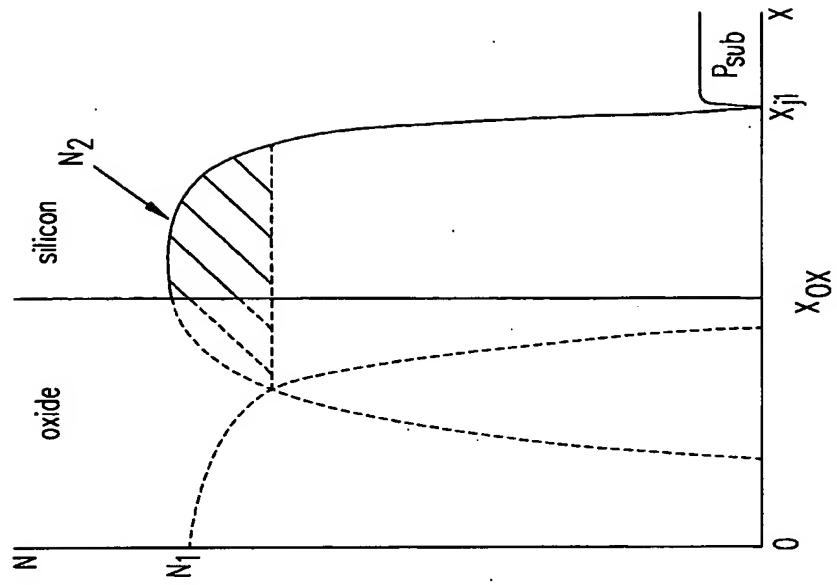


FIG. 17F

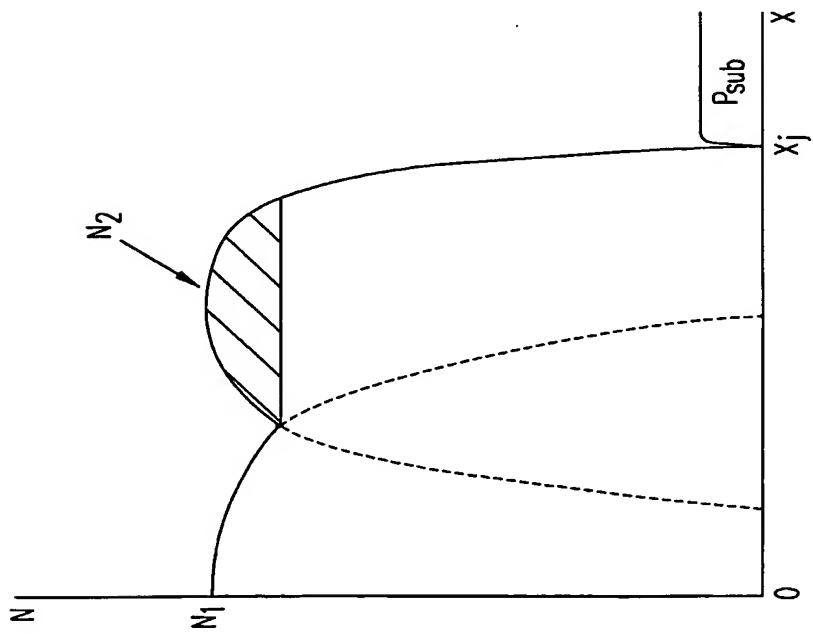
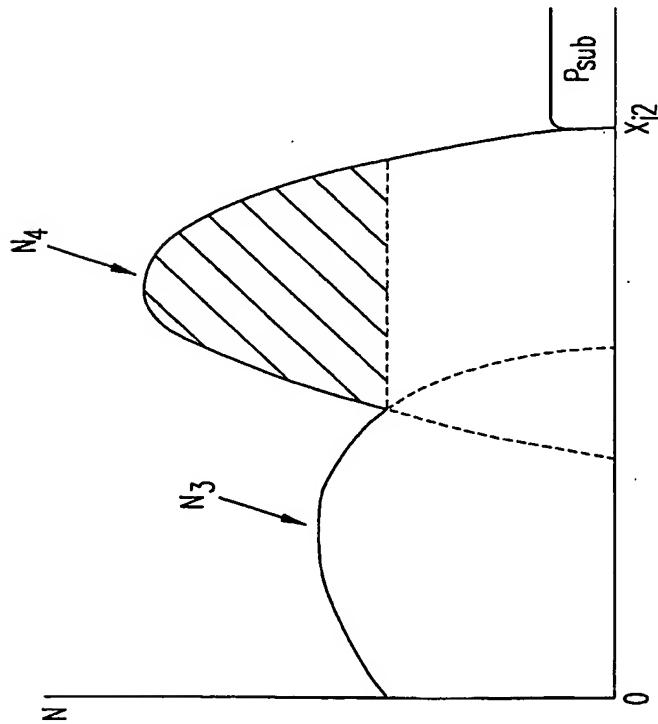
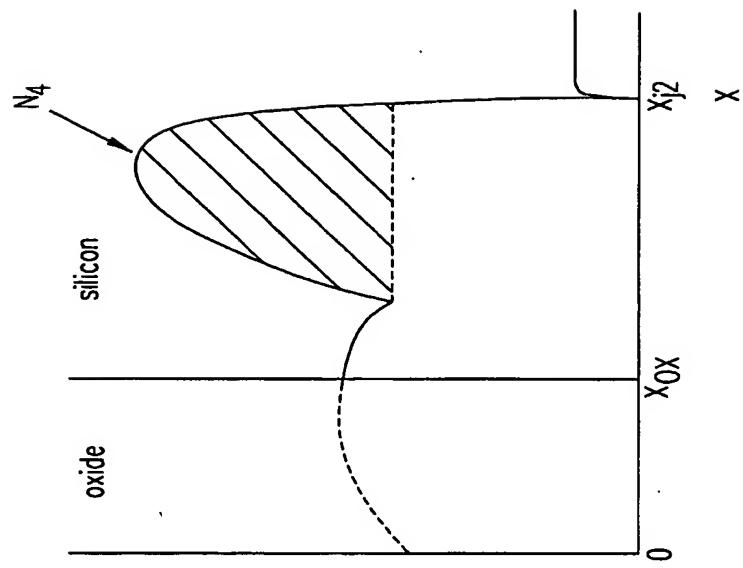


FIG. 17E

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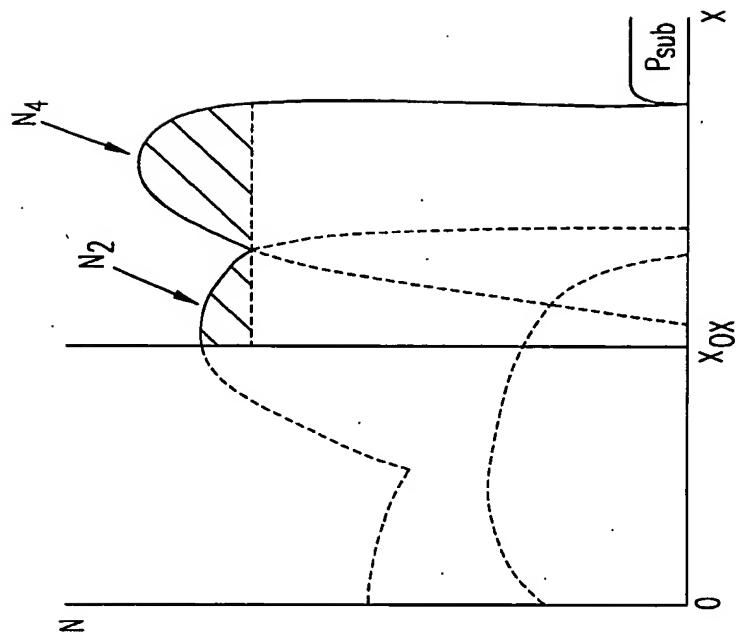


FIG. 17J

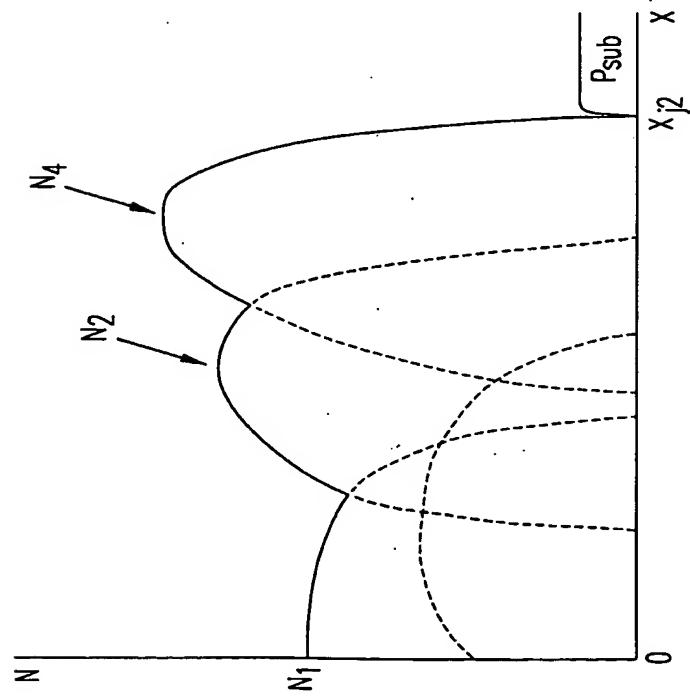


FIG. 17I

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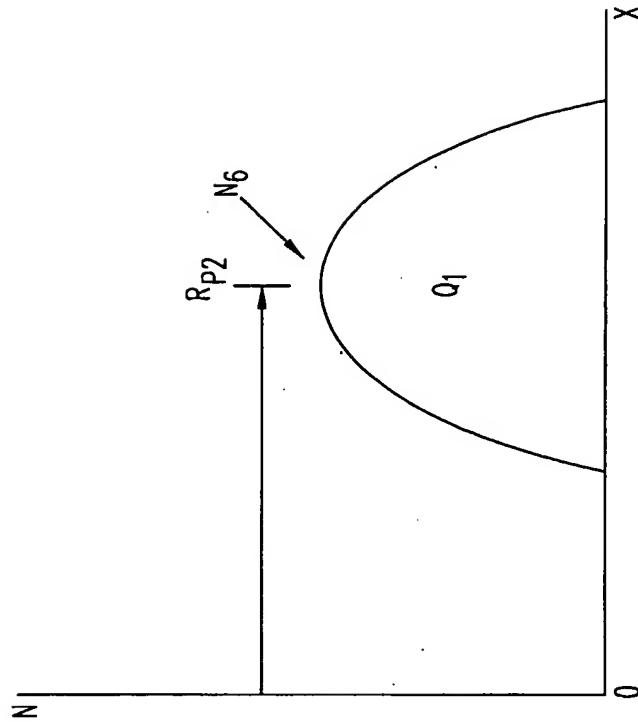


FIG. 17L
(Prior Art)

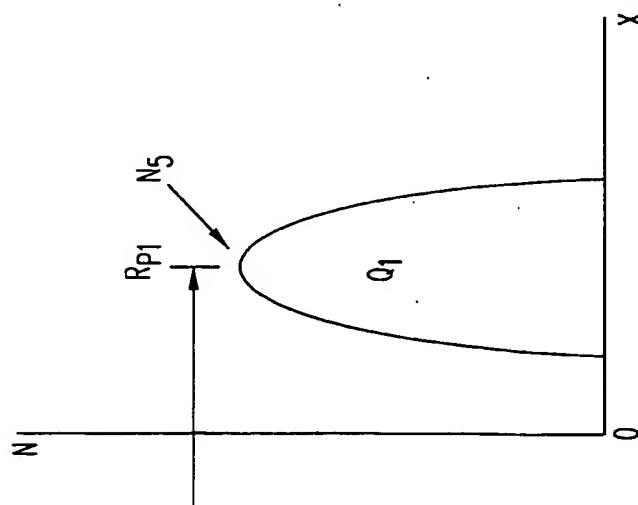


FIG. 17K
(Prior Art)

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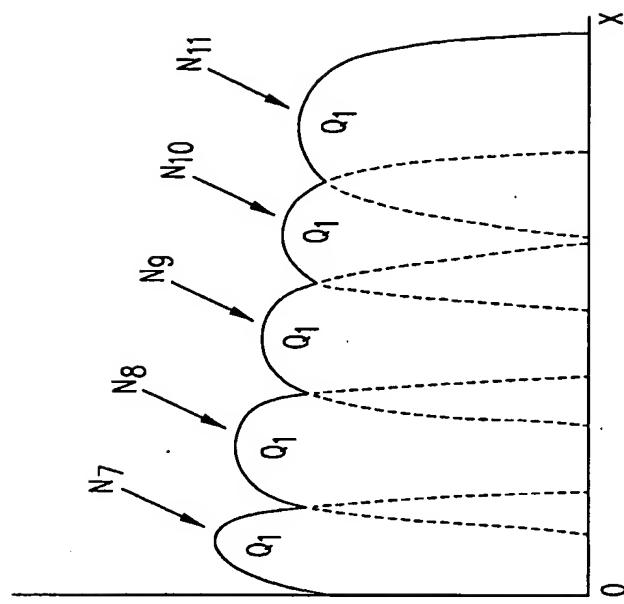


FIG. 17N

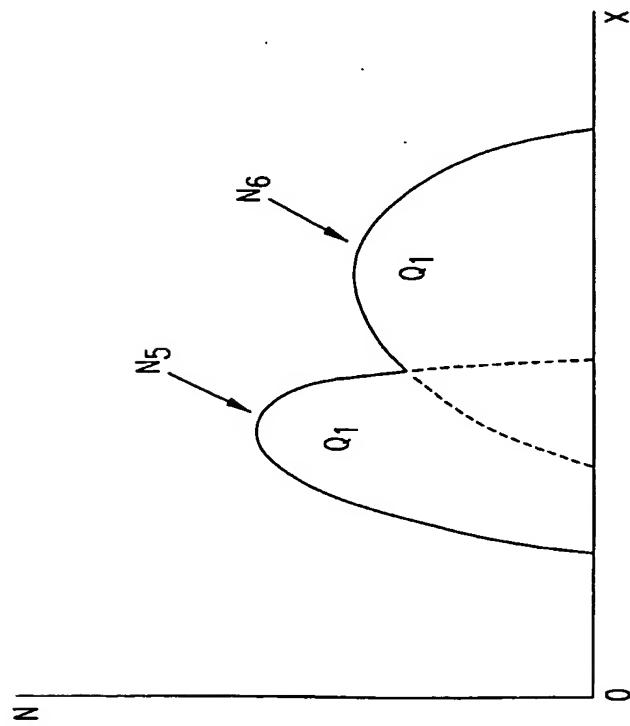


FIG. 17M

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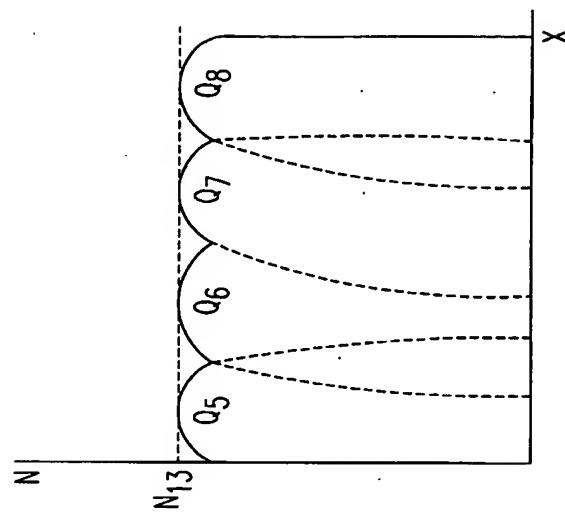


FIG. 17P

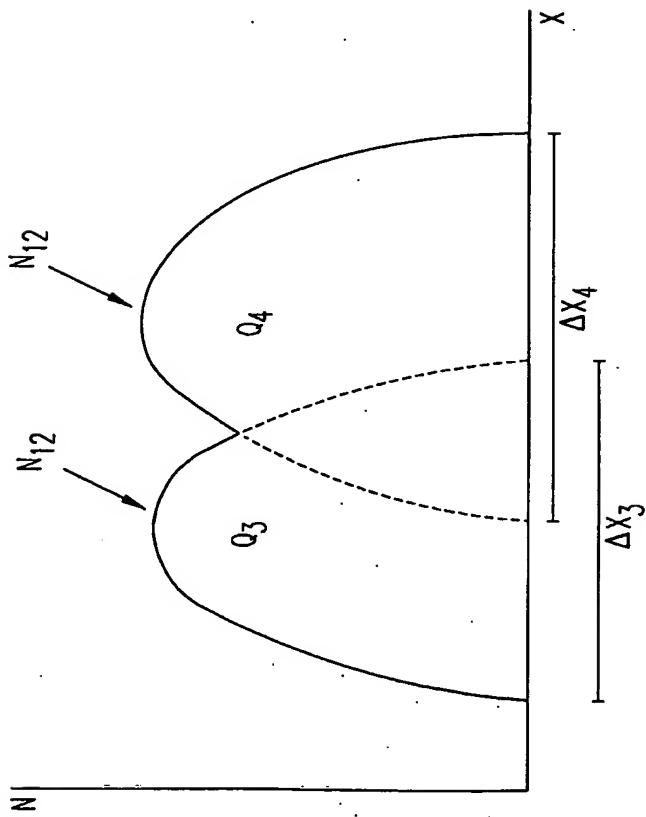


FIG. 17O

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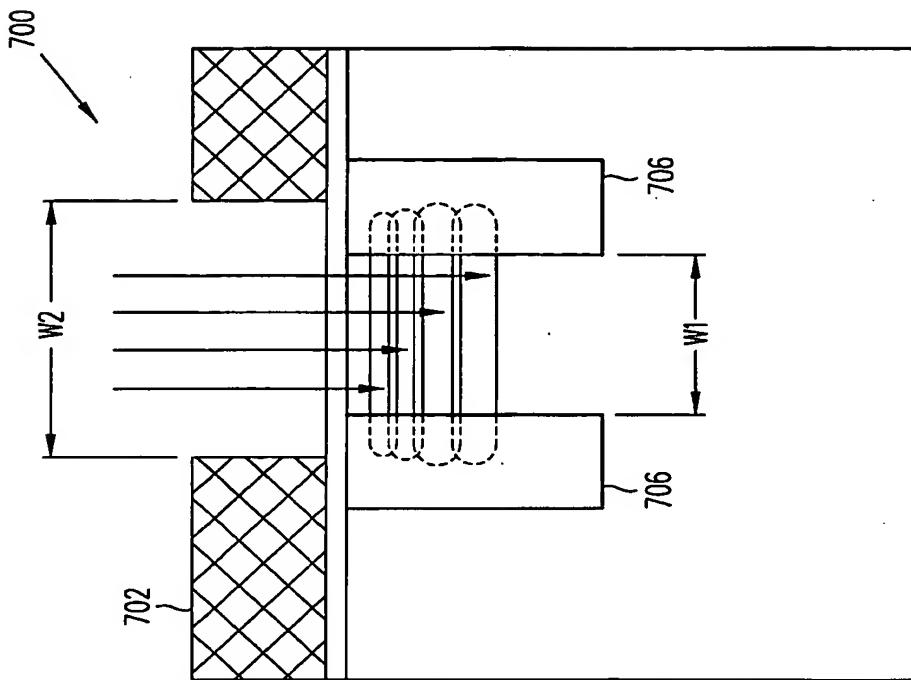


FIG. 17R

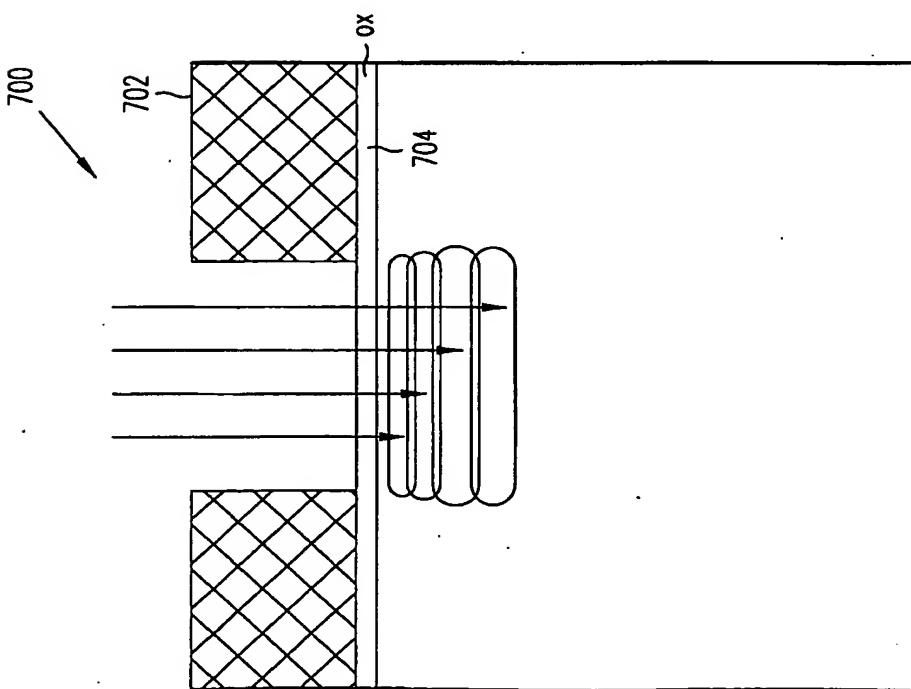


FIG. 17Q

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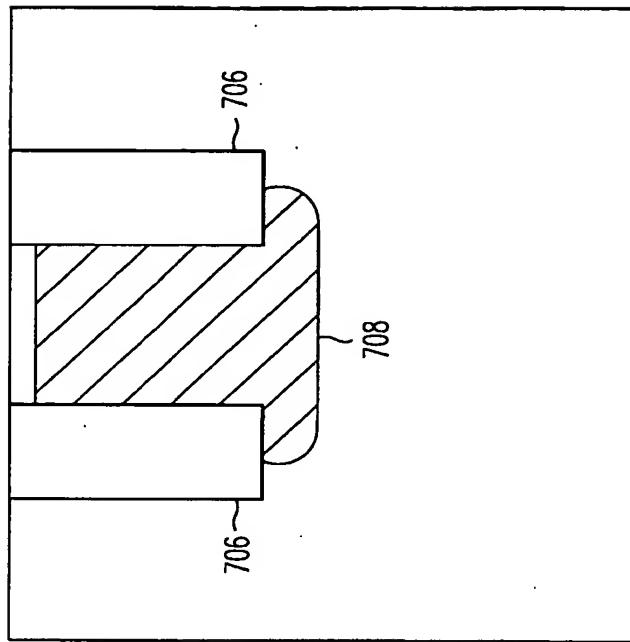


FIG. 17T

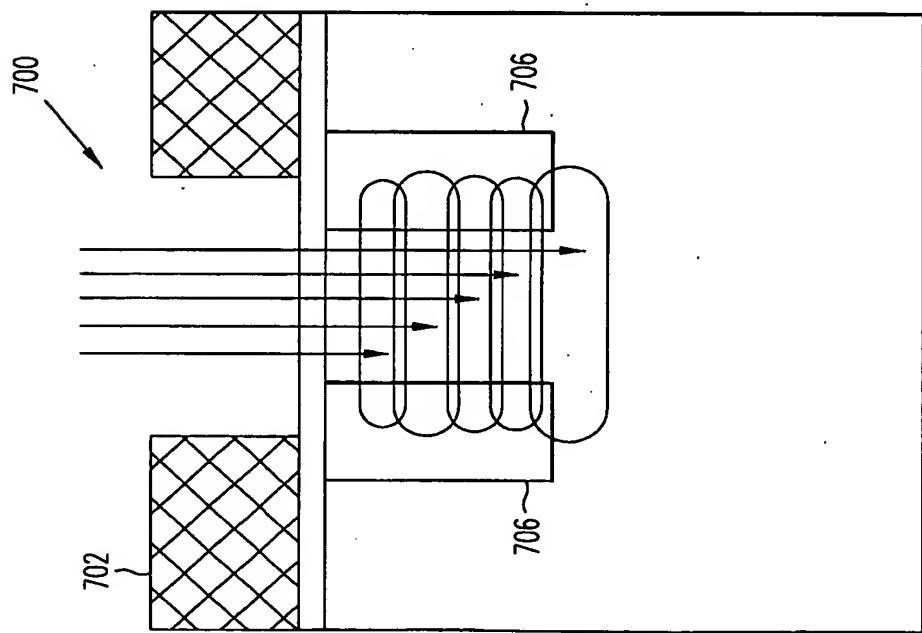
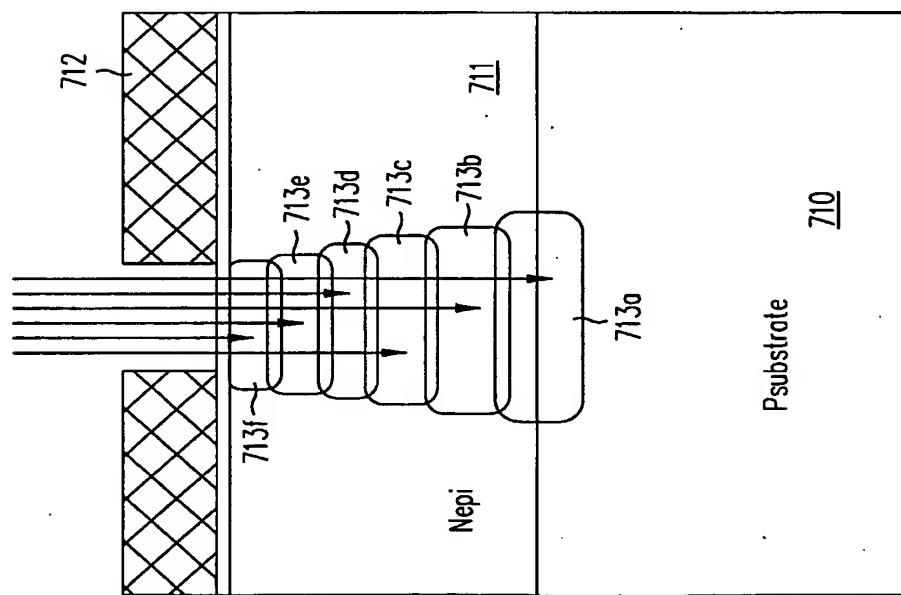
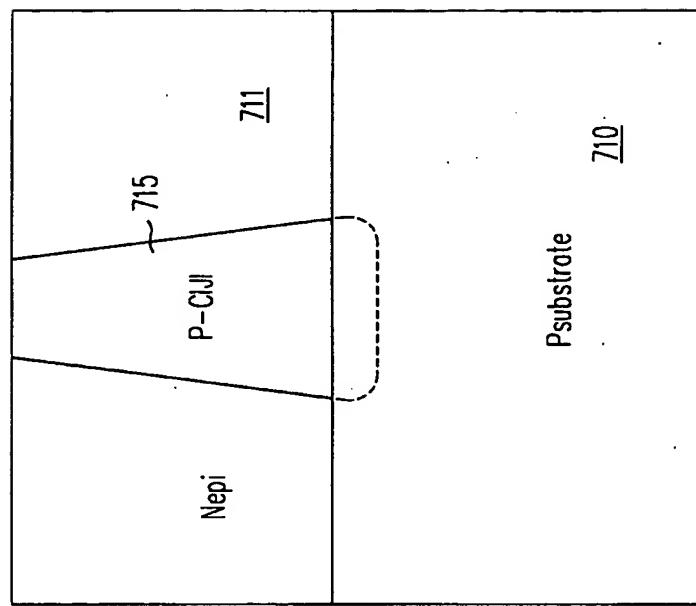
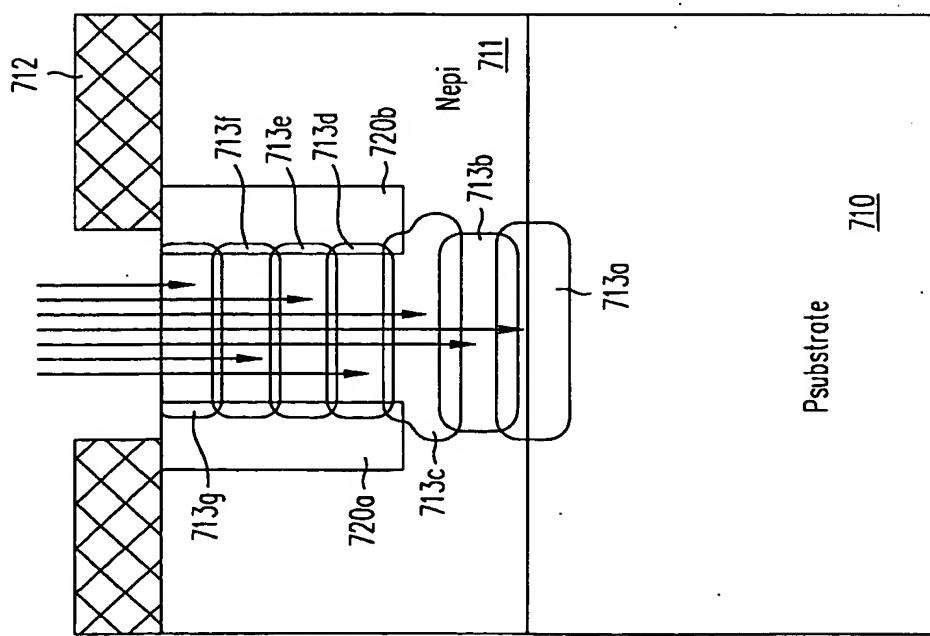
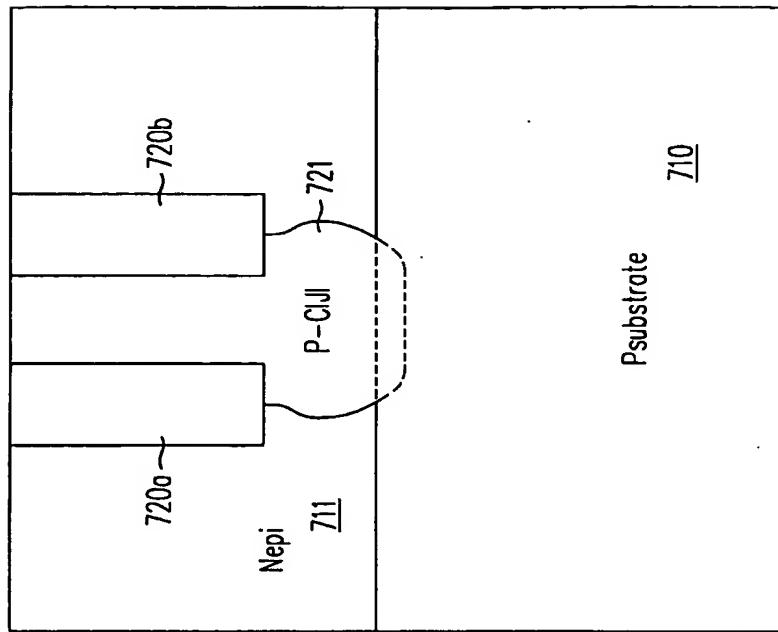


FIG. 17S





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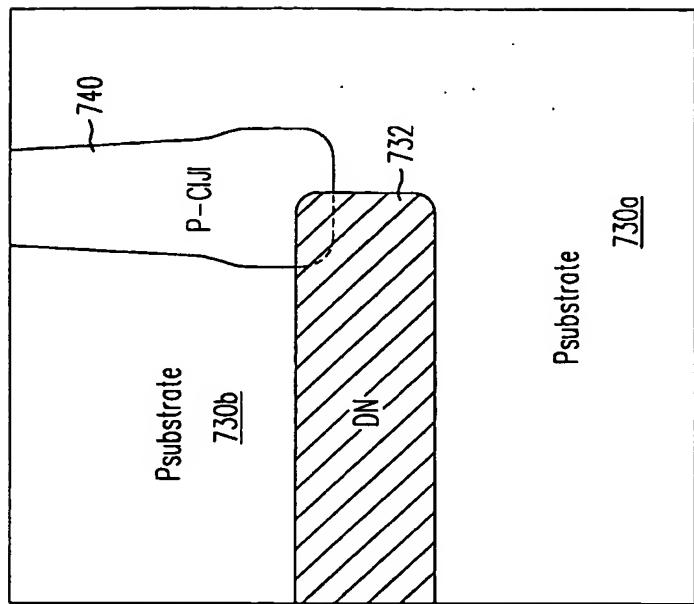


FIG. 17Z

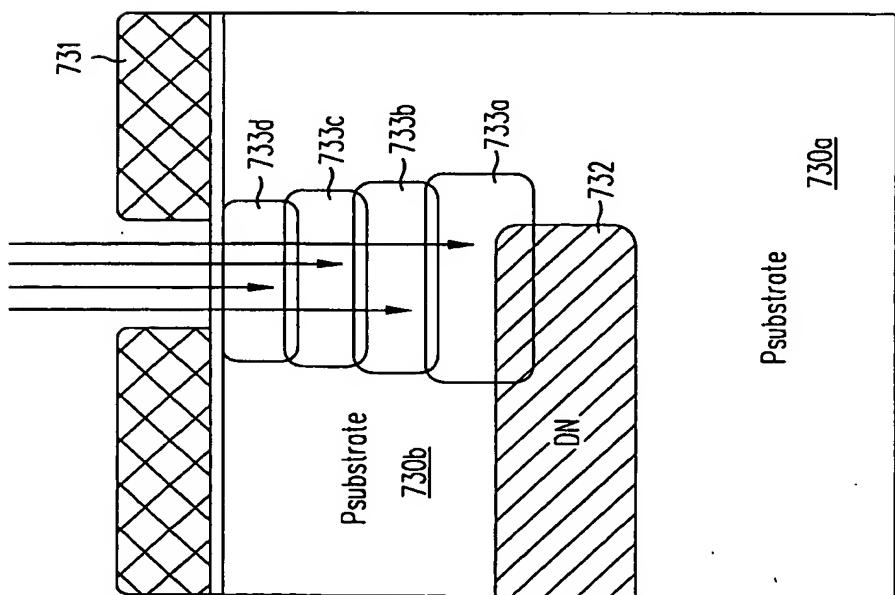
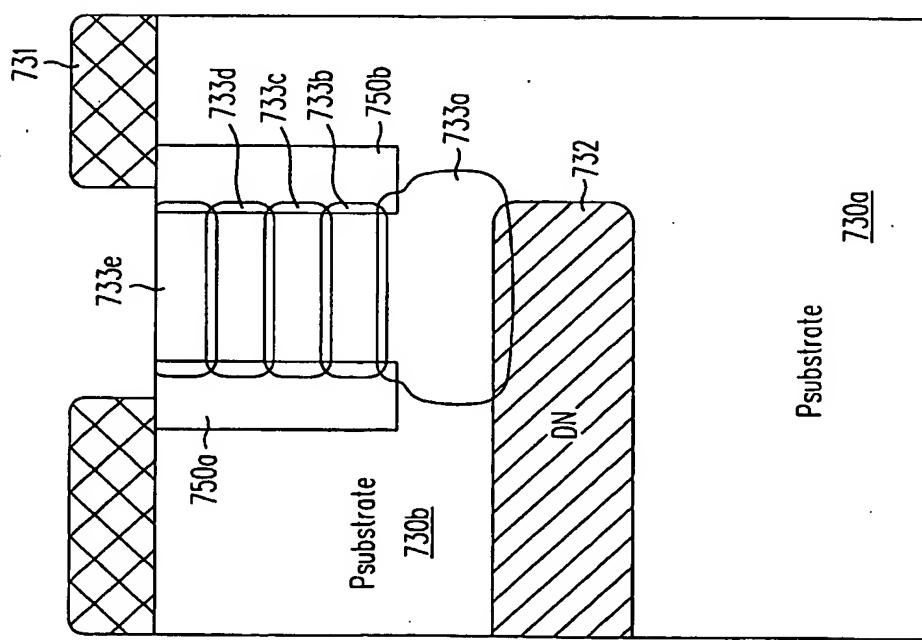
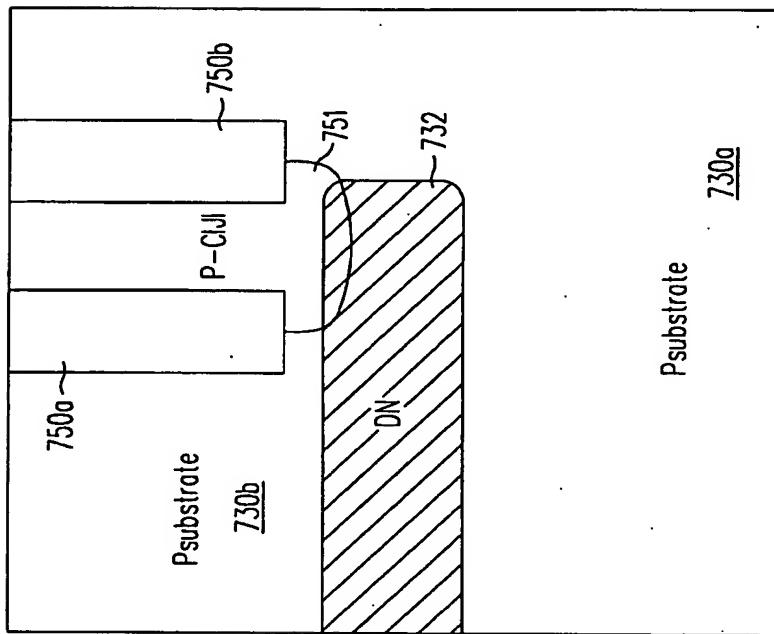


FIG. 17Y



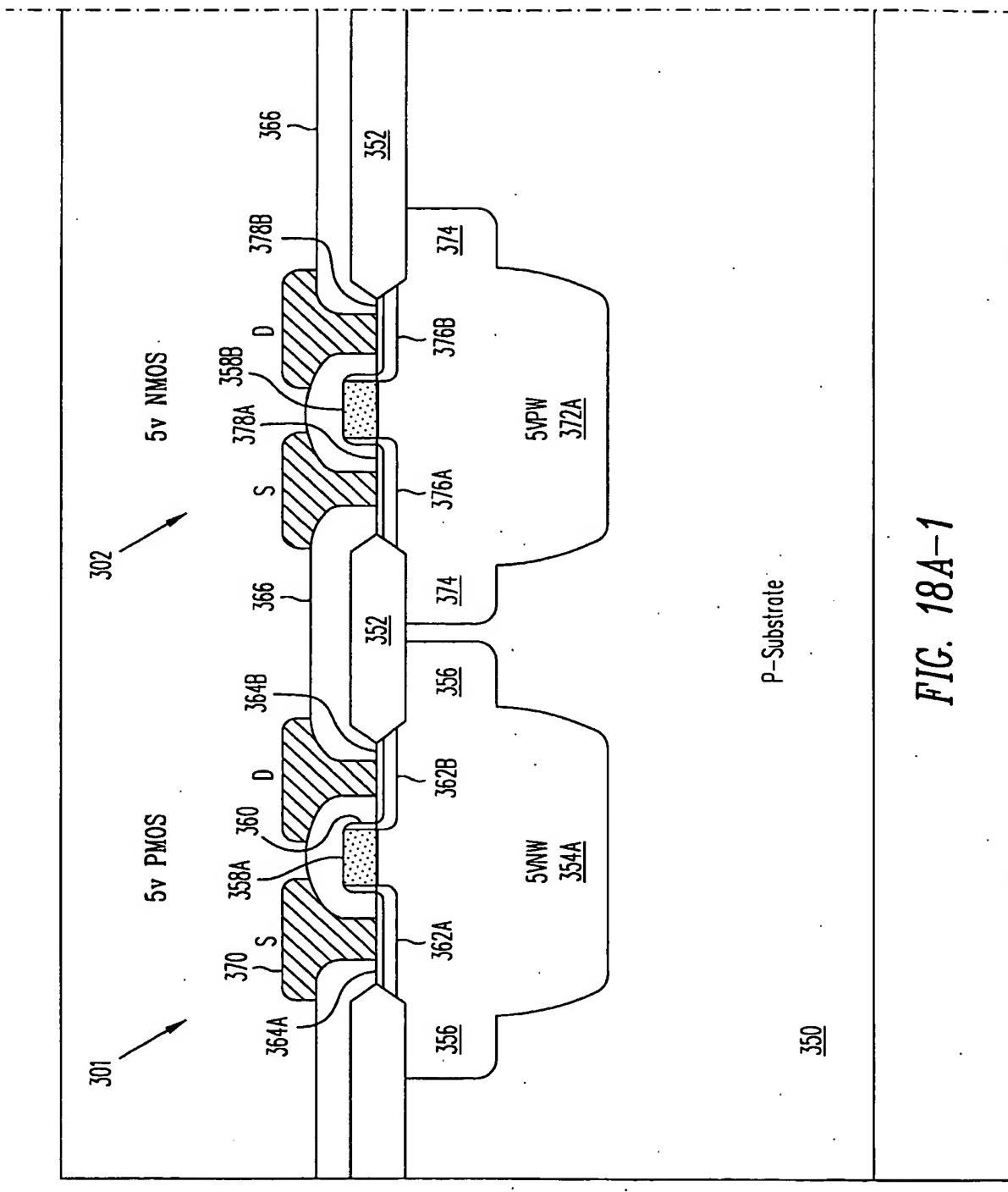


FIG. 18A-1	FIG. 18A-2
FIG. 18A-3	FIG. 18A-4

Key To

FIG. 18A

FIG. 18A-1

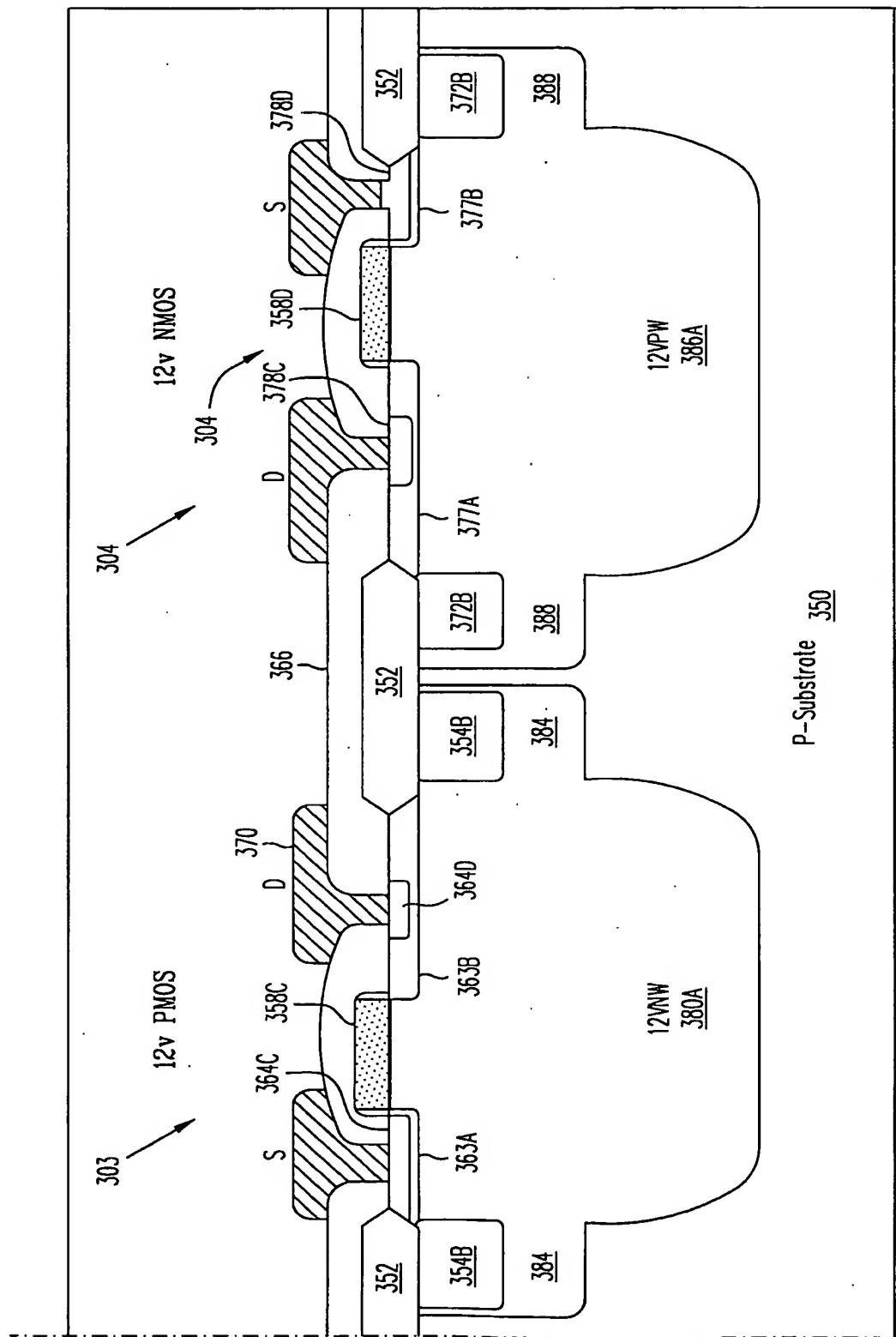


FIG. 18A-2

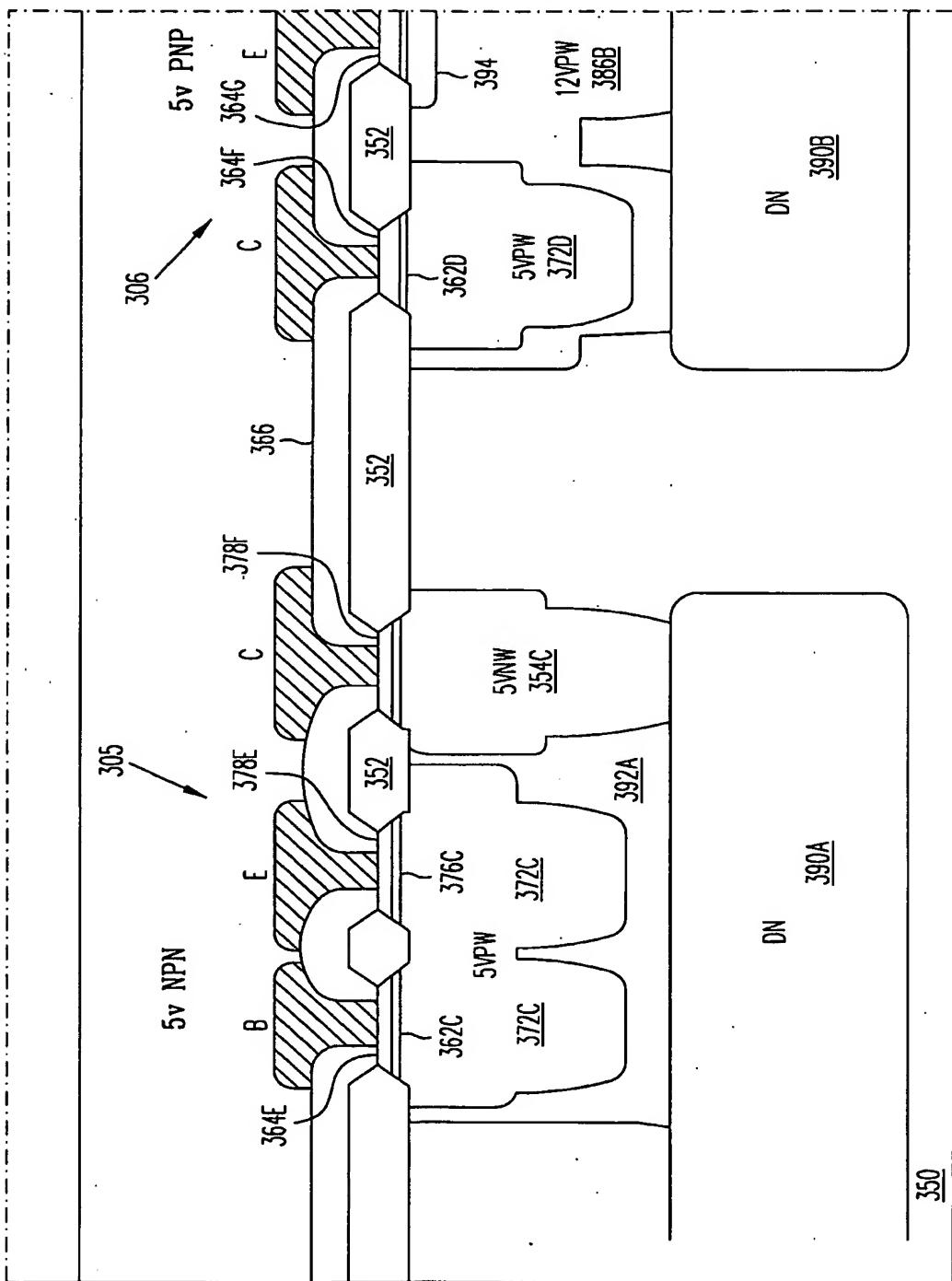


FIG. 18A-3

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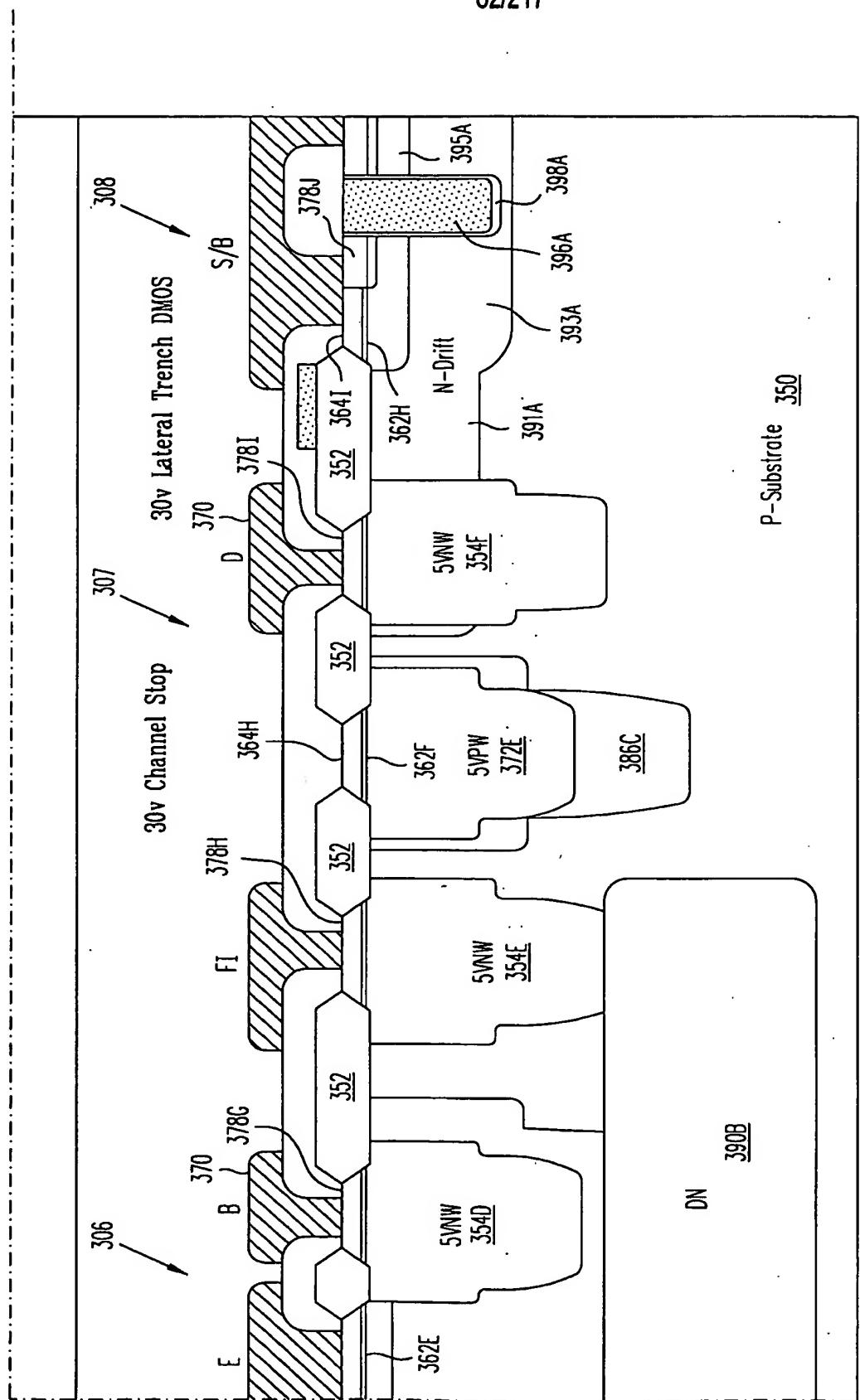


FIG. 18A-4

FIG. 18B-1

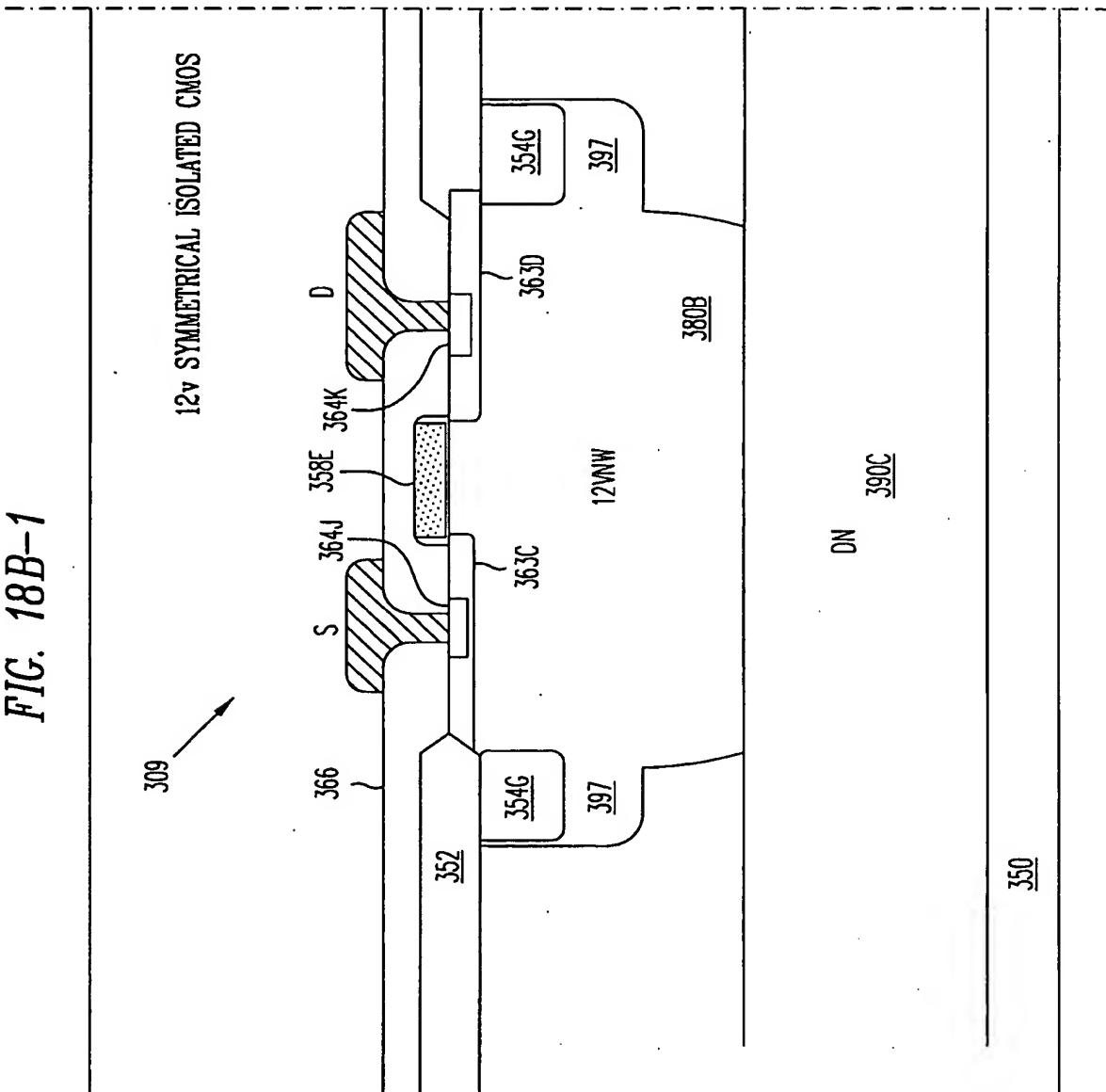
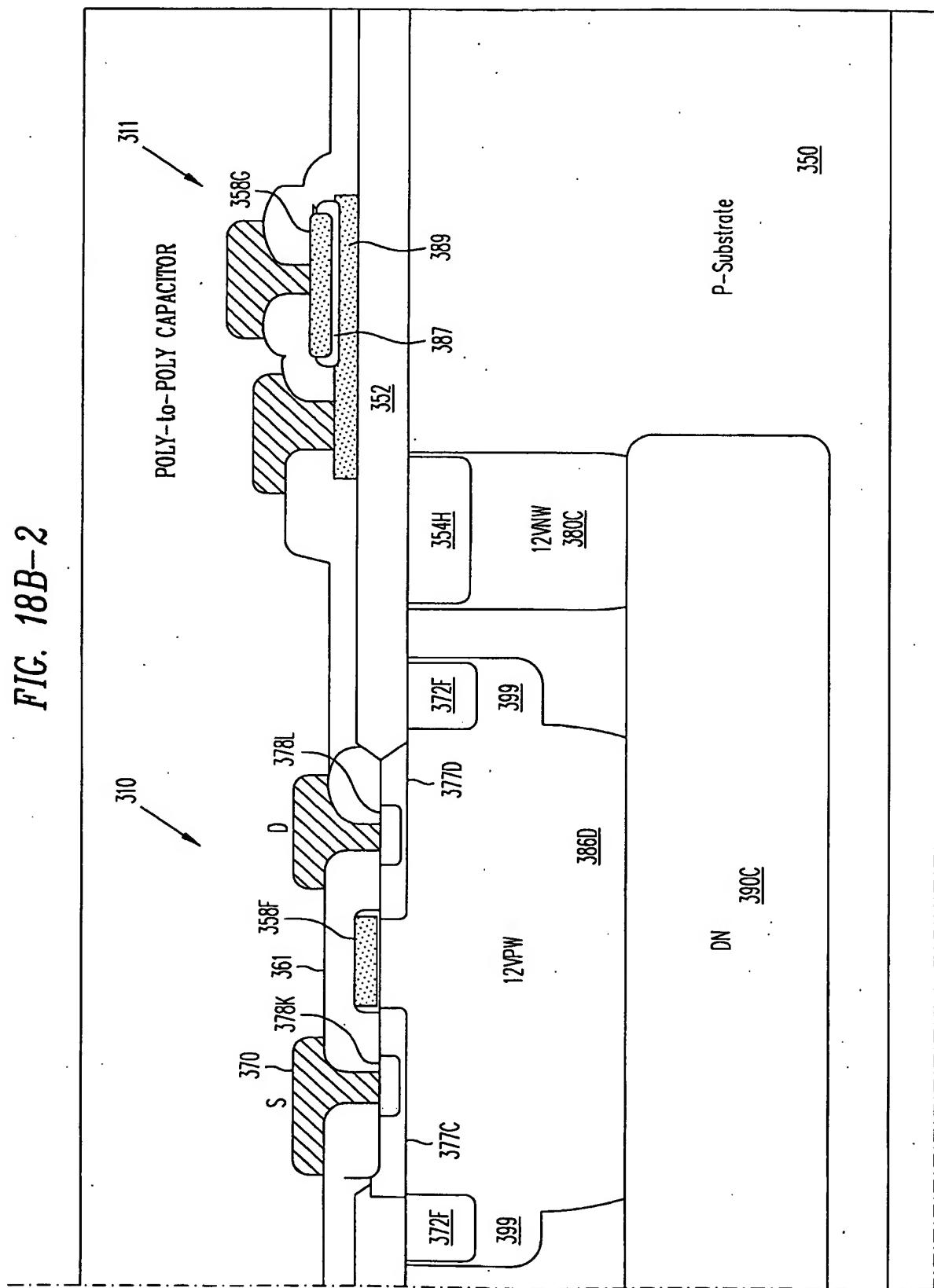


FIG. 18B-1	FIG. 18B-2
FIG. 18B-3	FIG. 18B-4

Key to
FIG. 18B

FIG. 18B-2



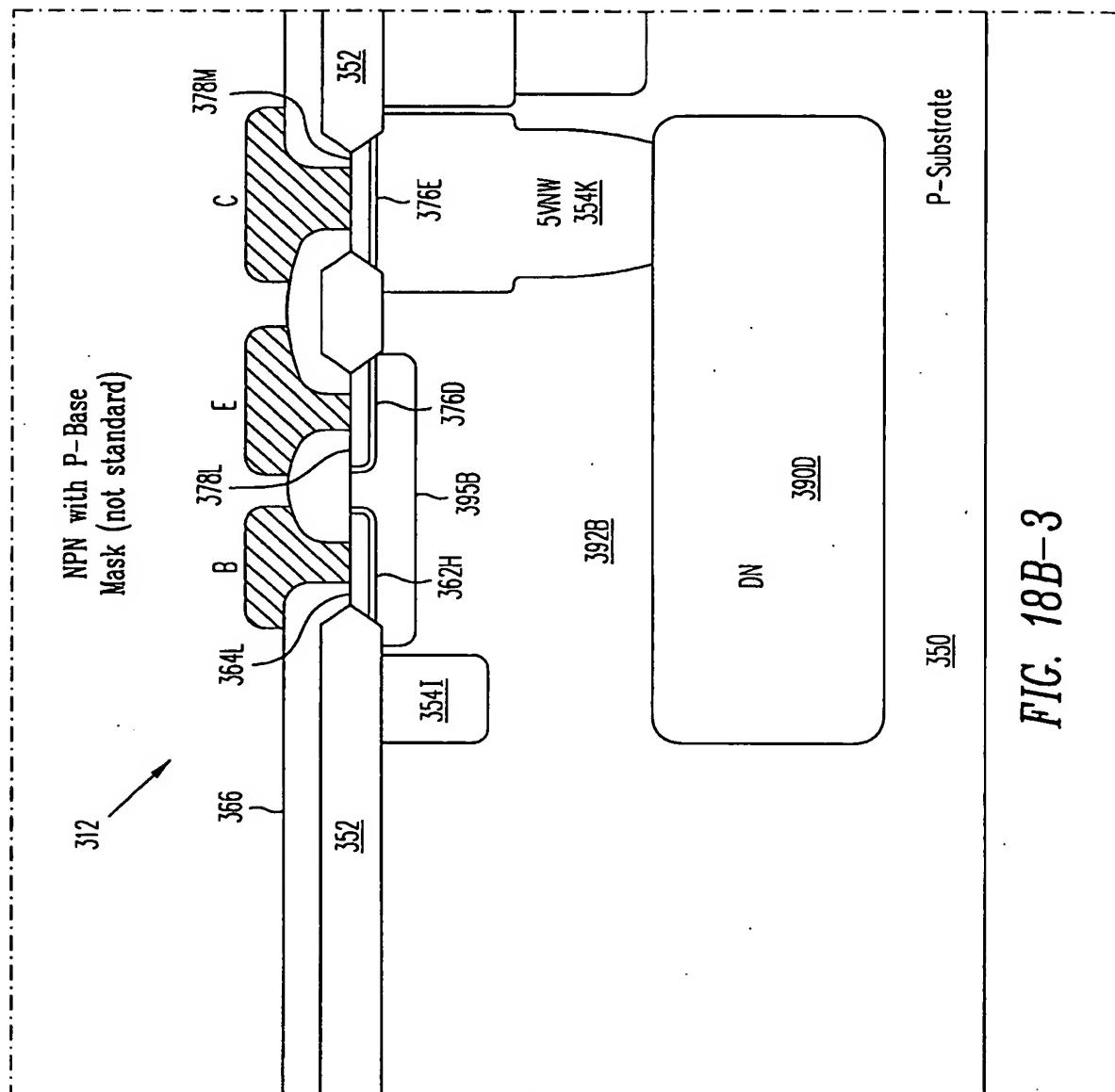


FIG. 18B-3

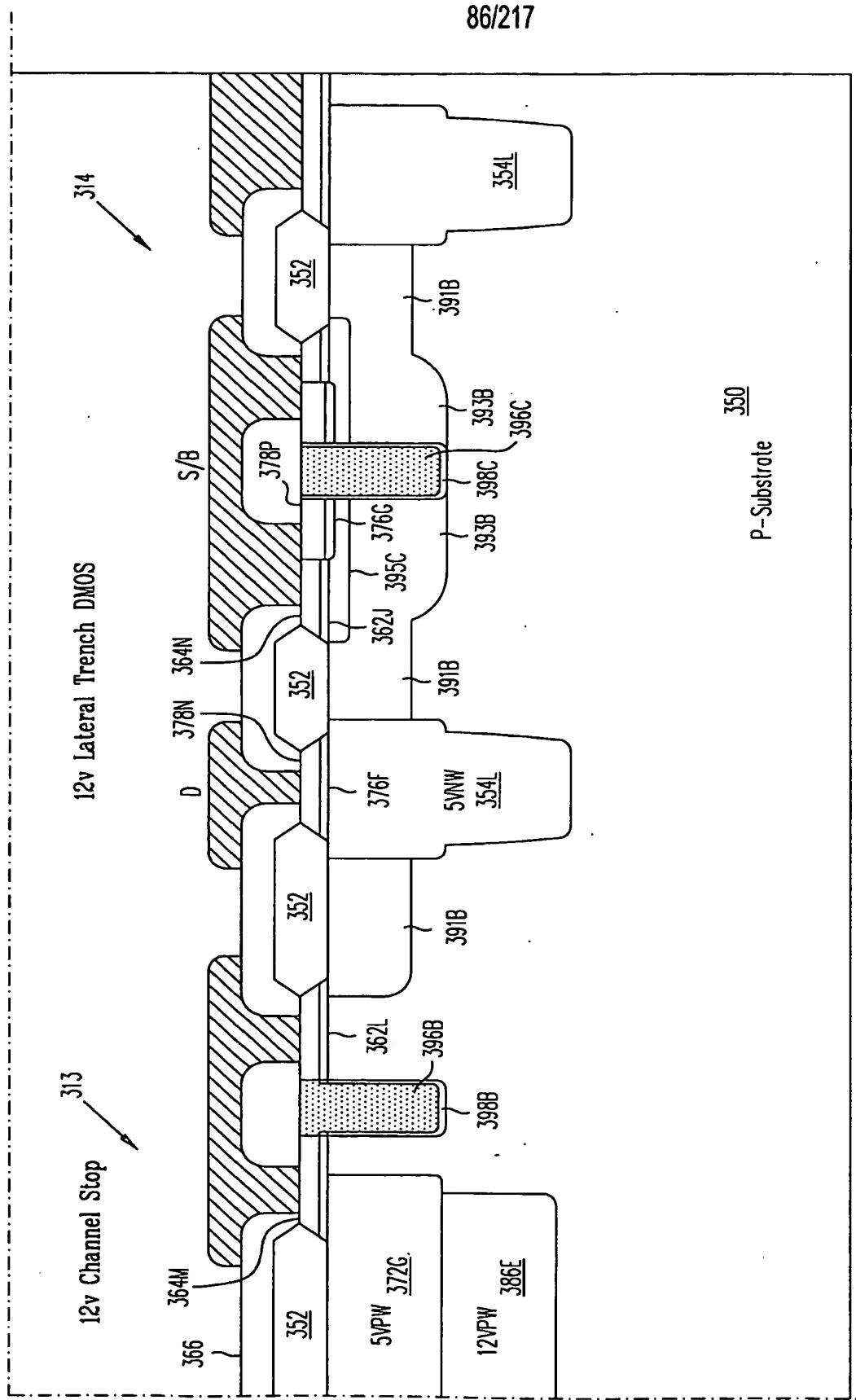


FIG. 18B-4

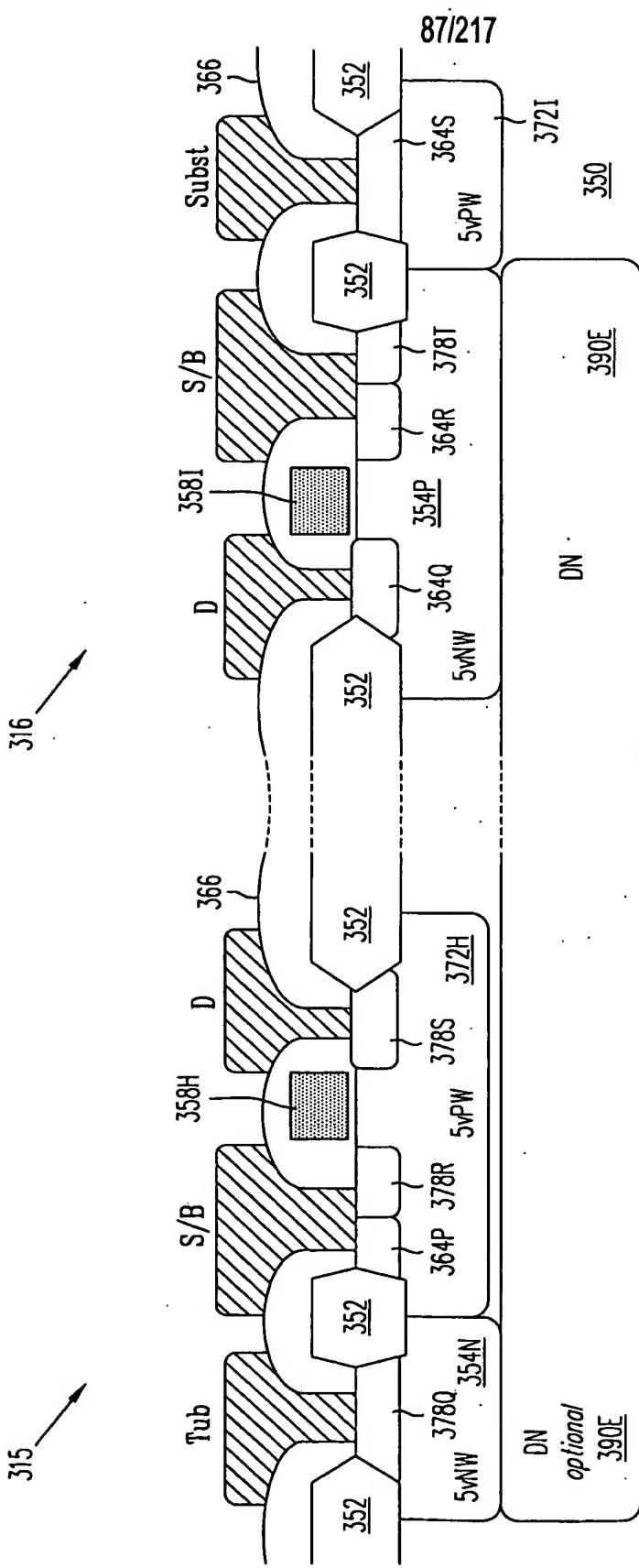
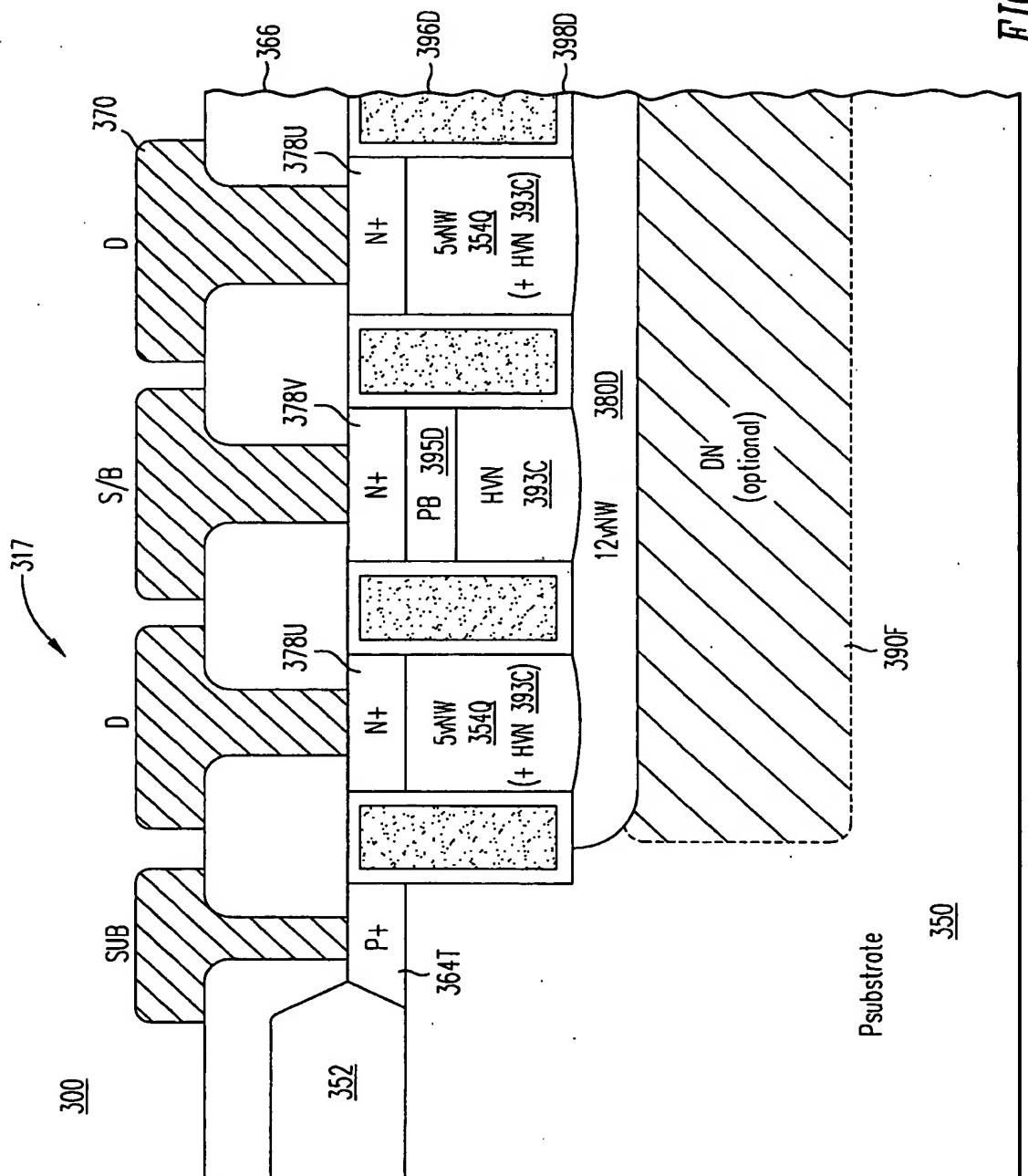


FIG. 18C



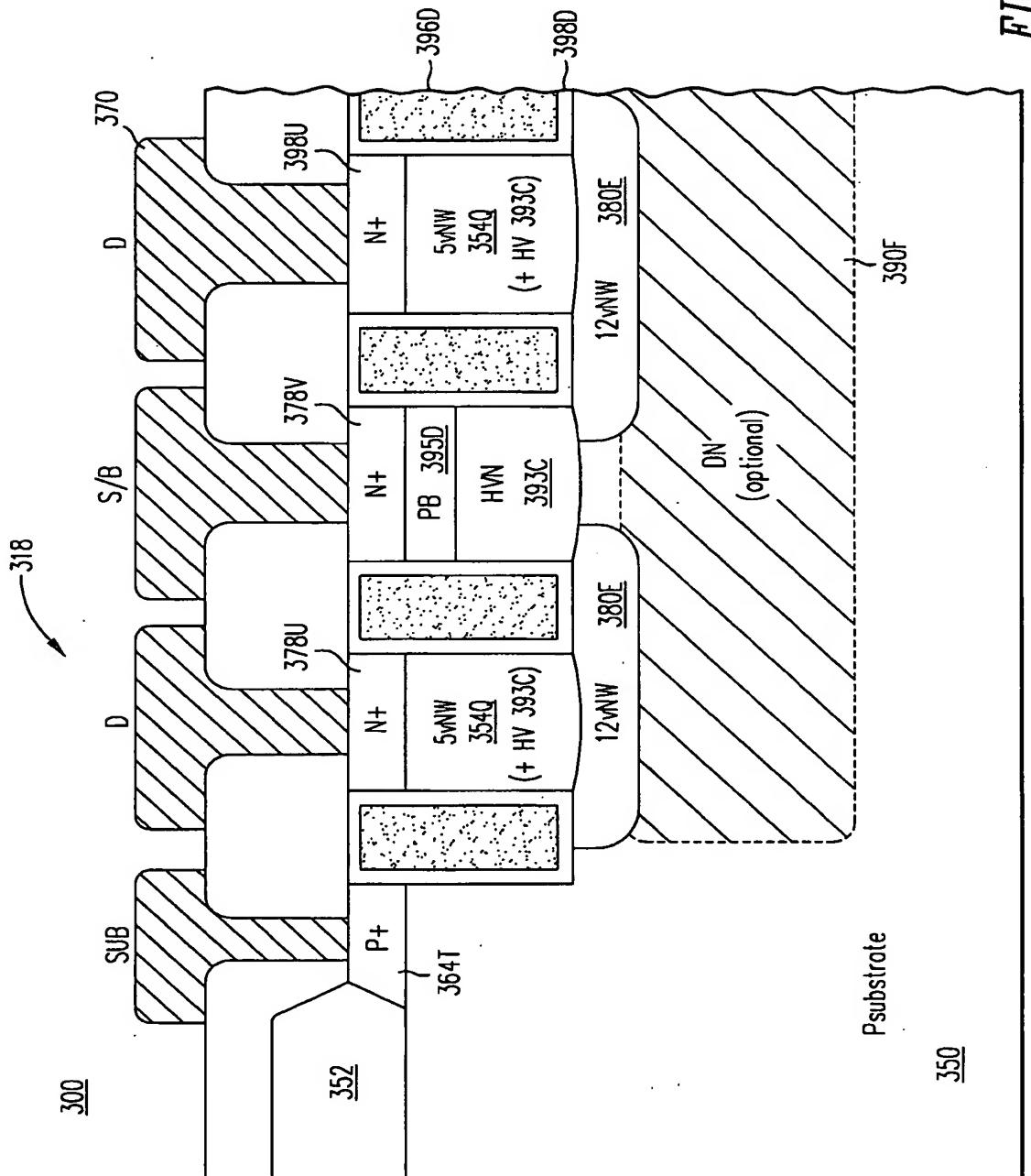


FIG. 18E

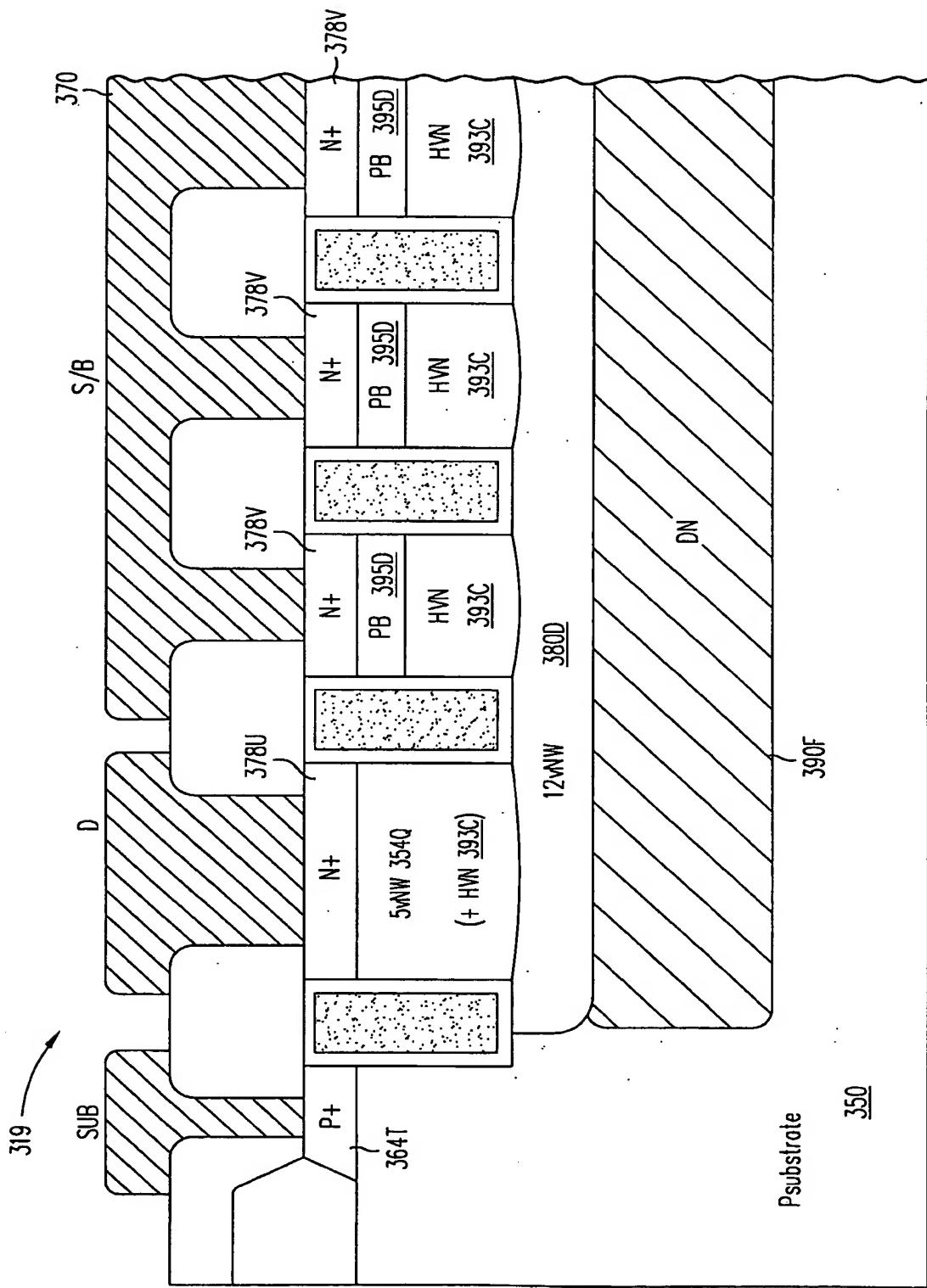


FIG. 18F

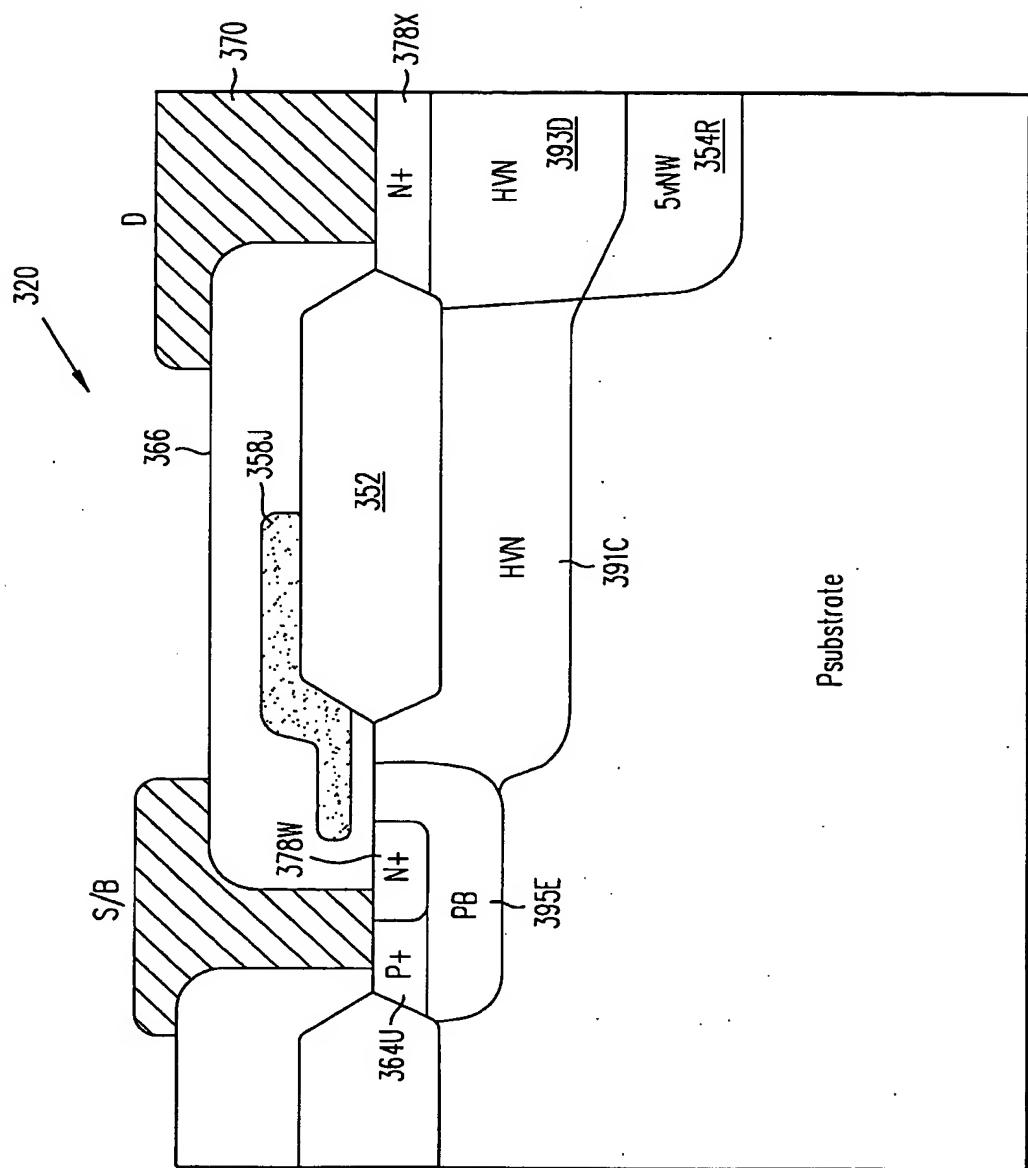


FIG. 18G

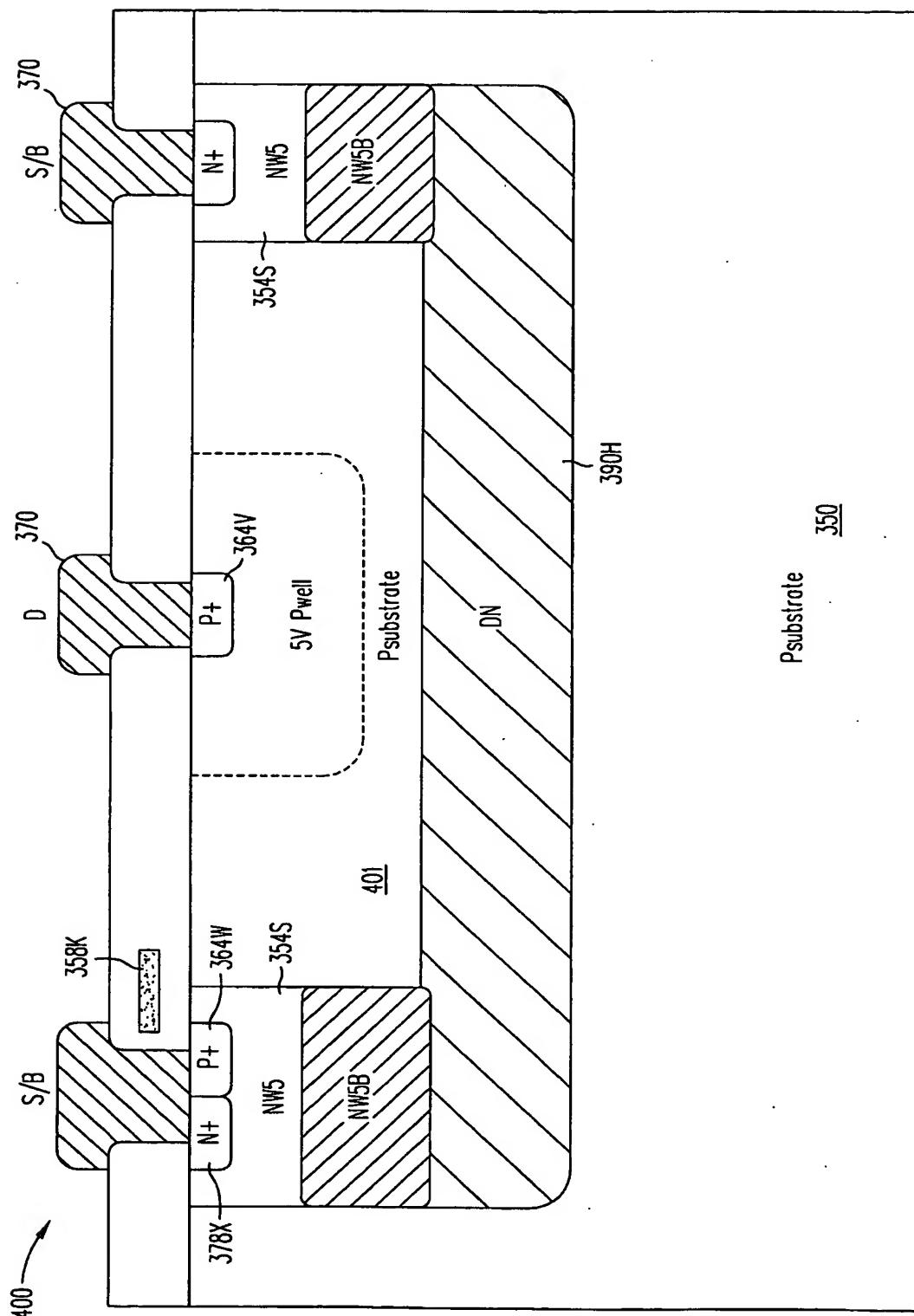
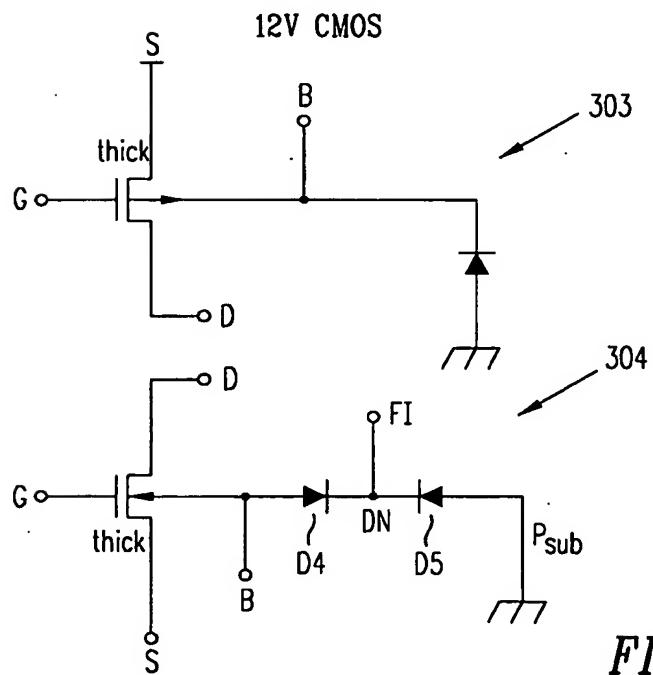
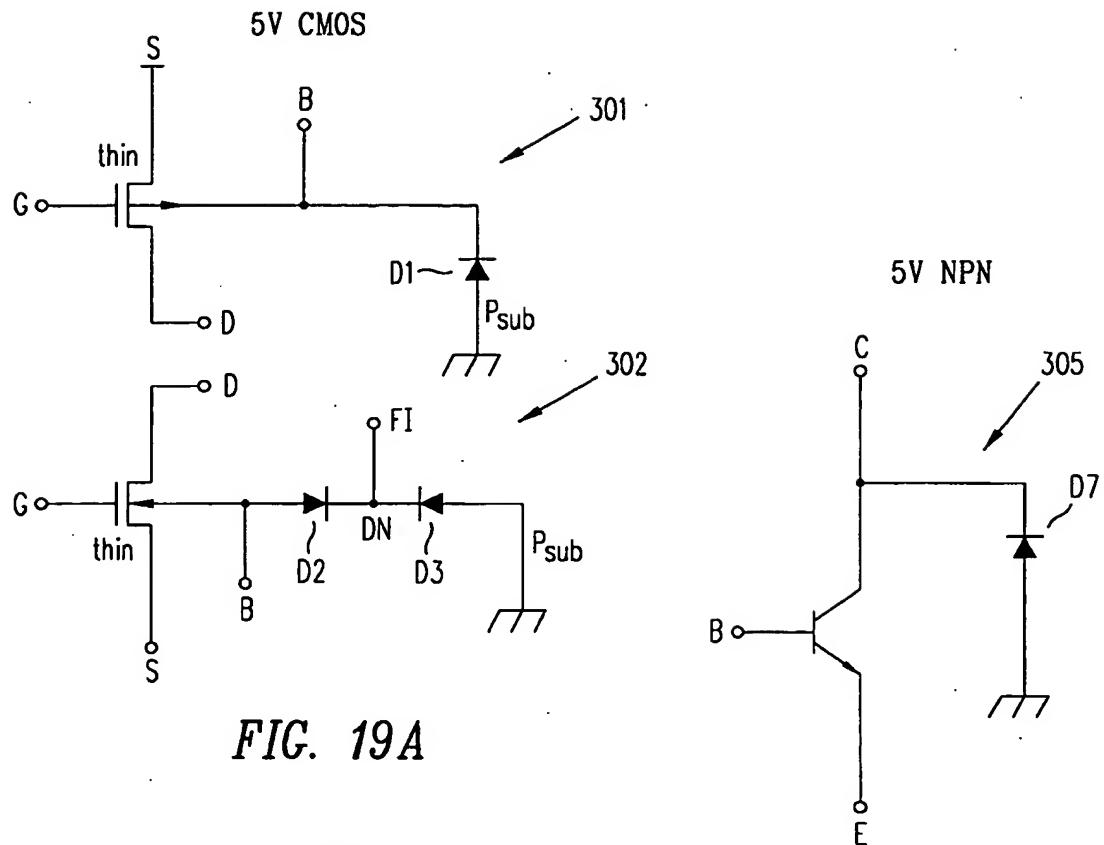


FIG. 18H



5V PNP

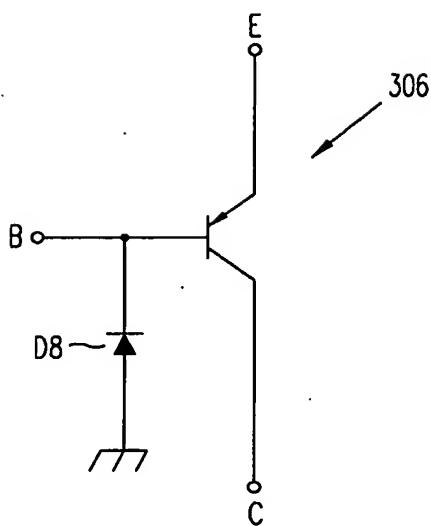


FIG. 19D

30V Trench LDMOS

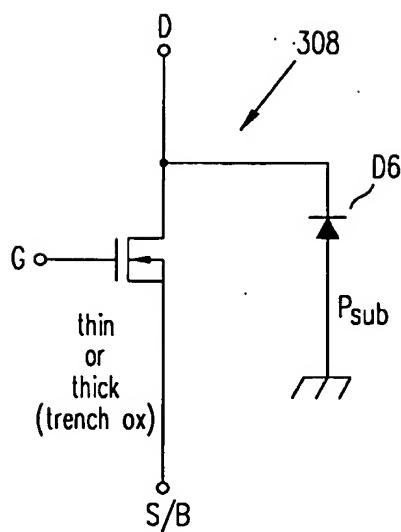


FIG. 19E

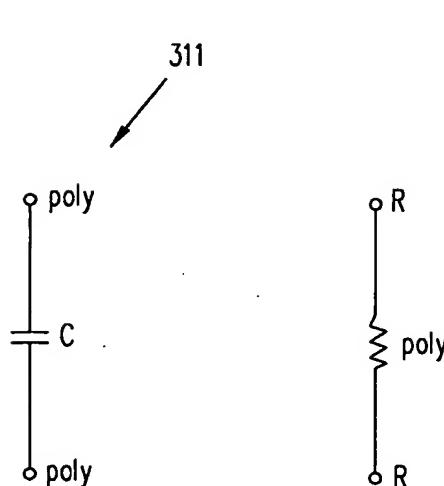


FIG. 19F

FIG. 19G

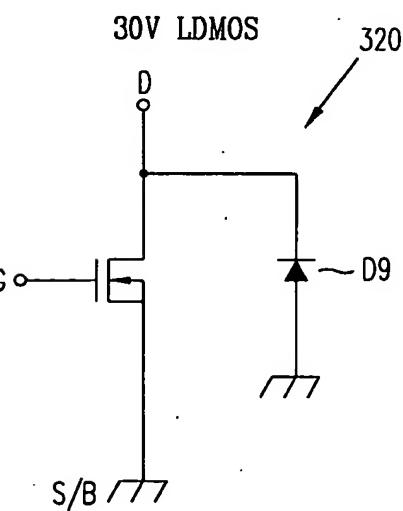
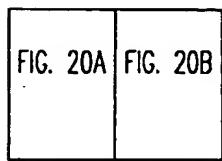
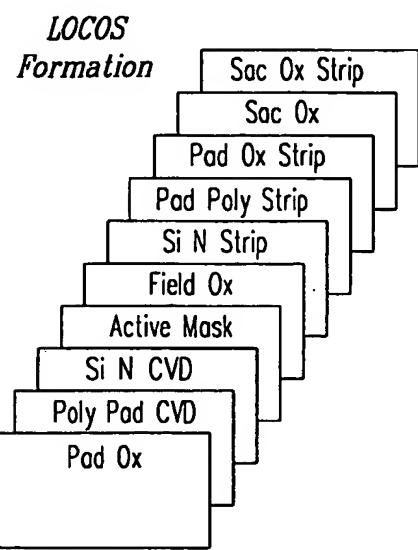


FIG. 19H



Key To
FIG. 20



hardmask

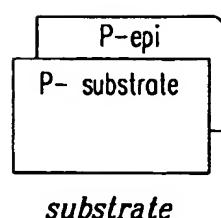
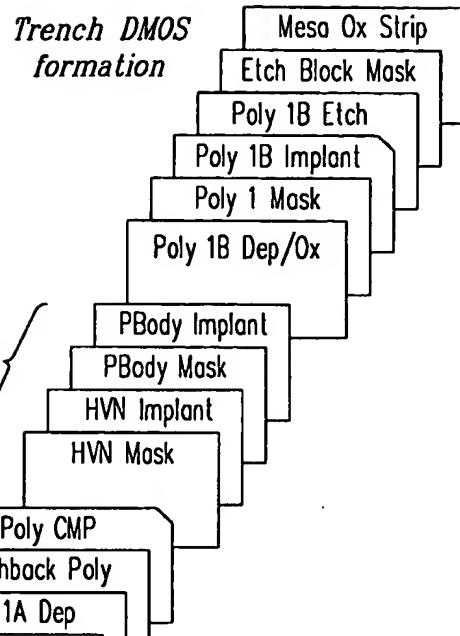
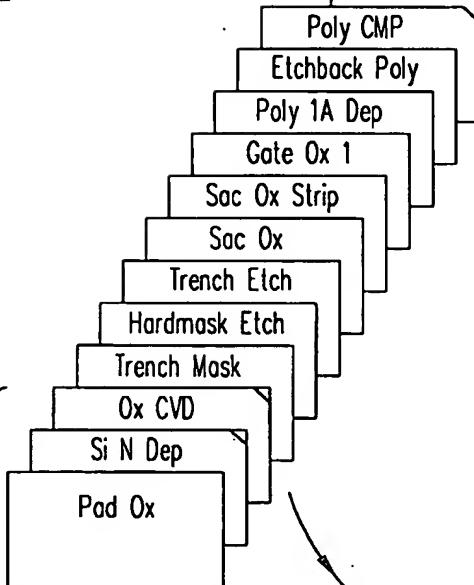


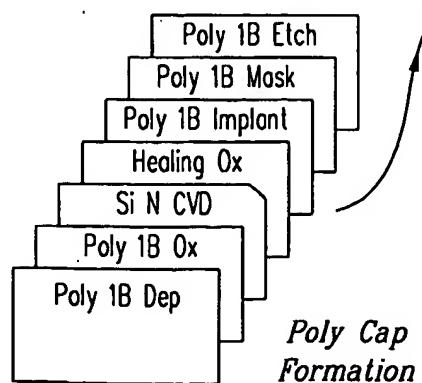
FIG. 20A



Doping



To
FIG. 20B



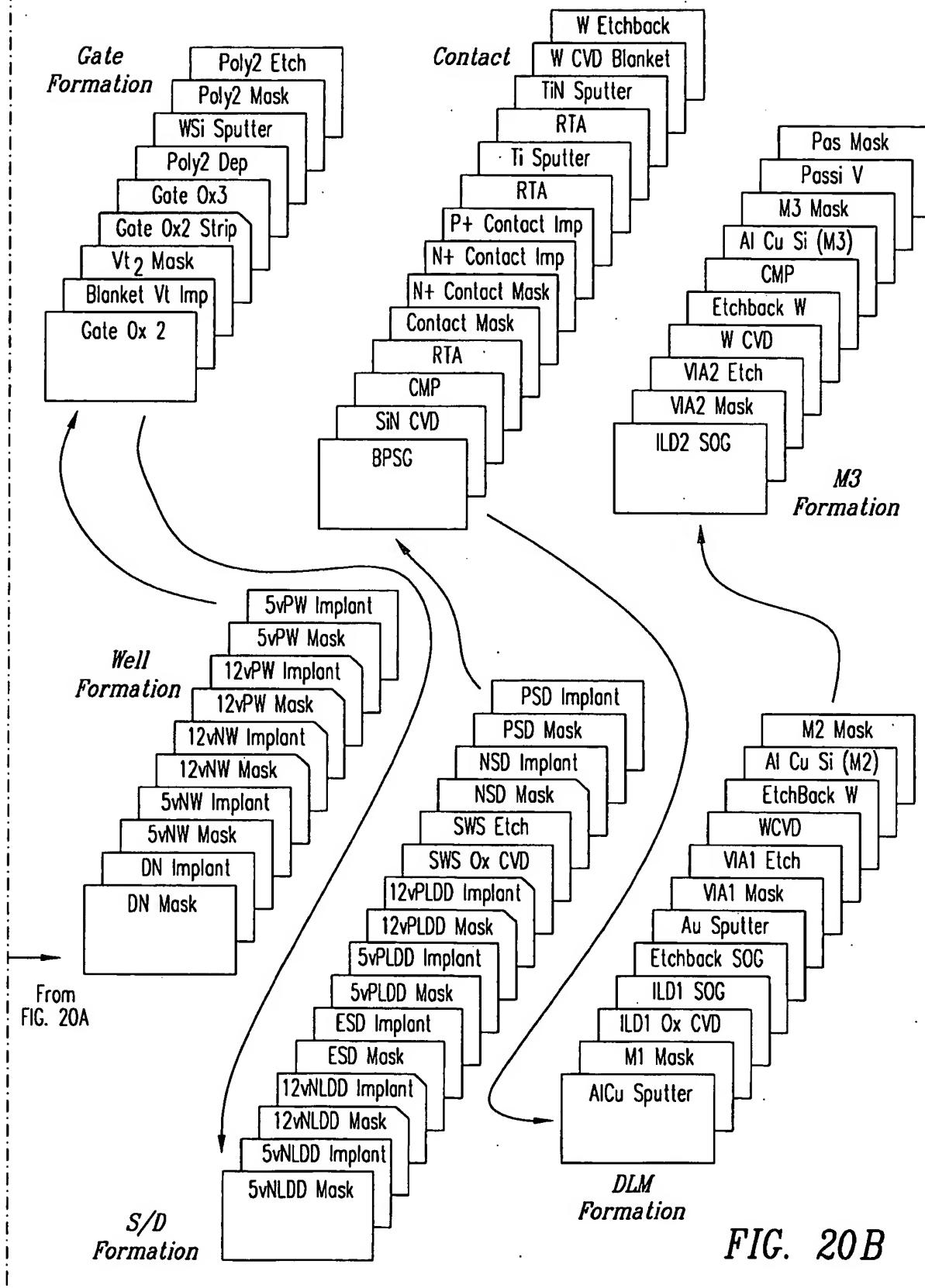
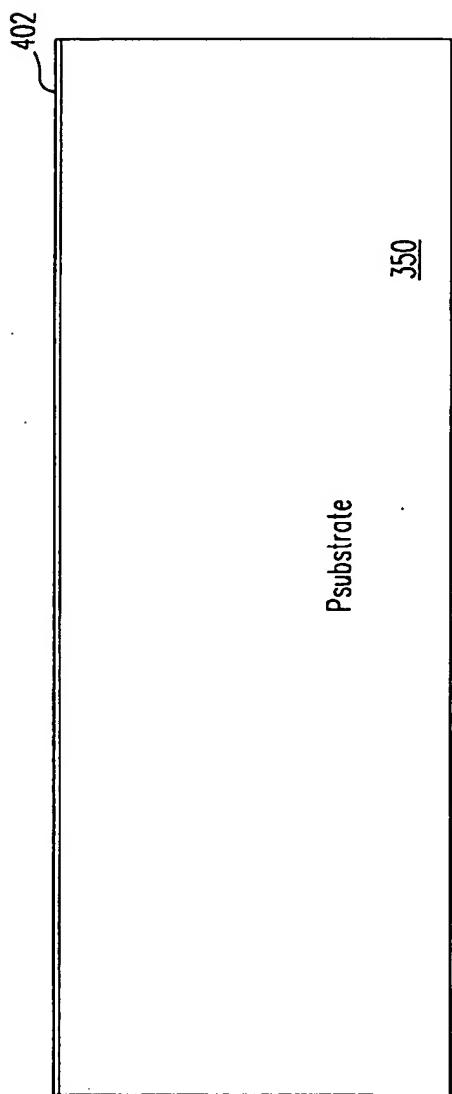


FIG. 20B

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FIG. 21



First Pad Oxide Layer

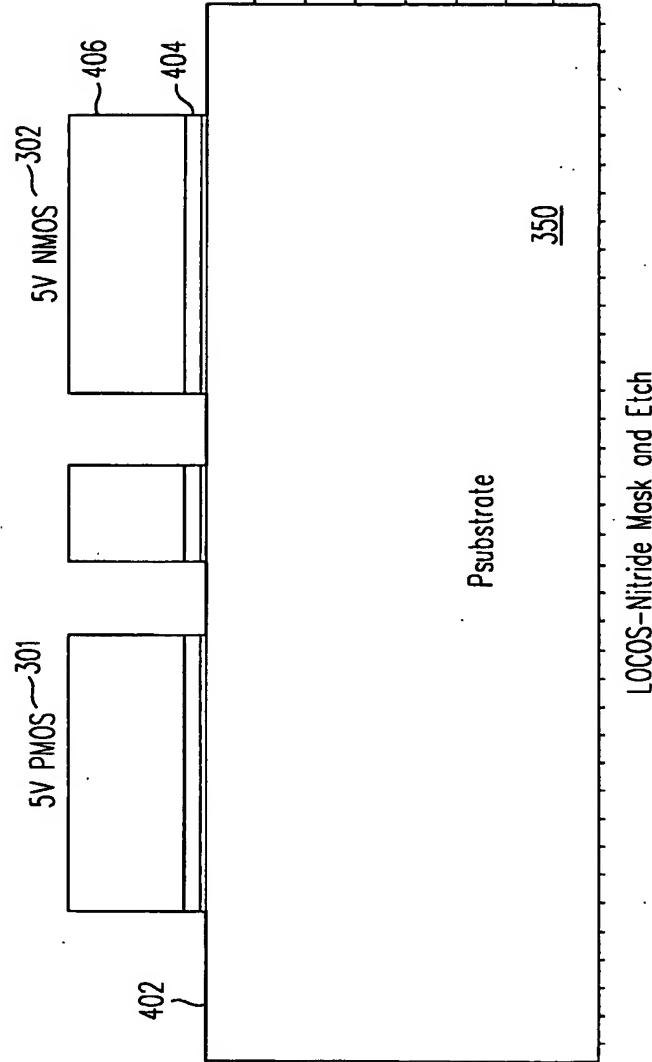


FIG. 22A

LOCOS-Nitride Mask and Etch

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FIG. 22B

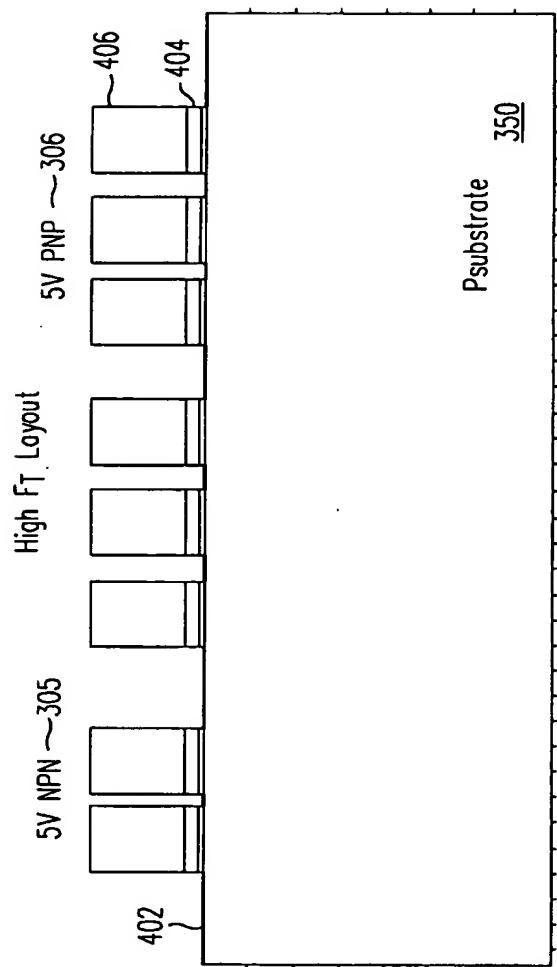


FIG. 22C

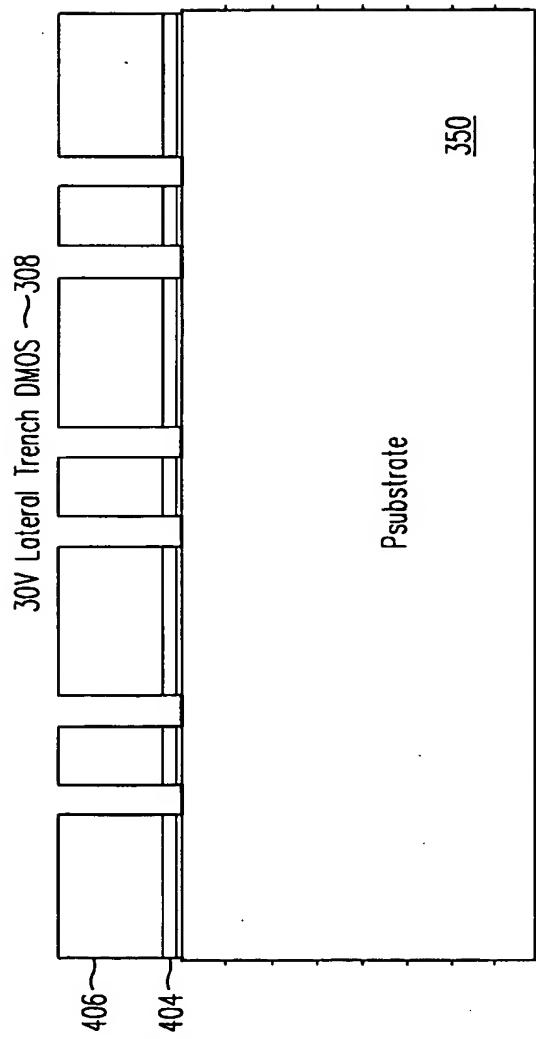


FIG. 22D

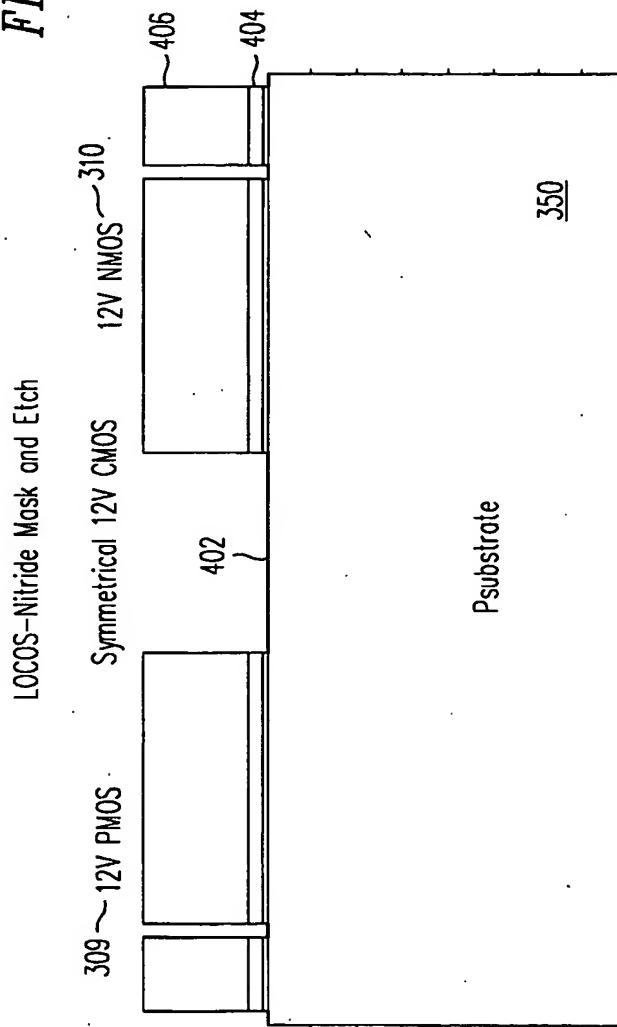


FIG. 22E

FIG. 23A

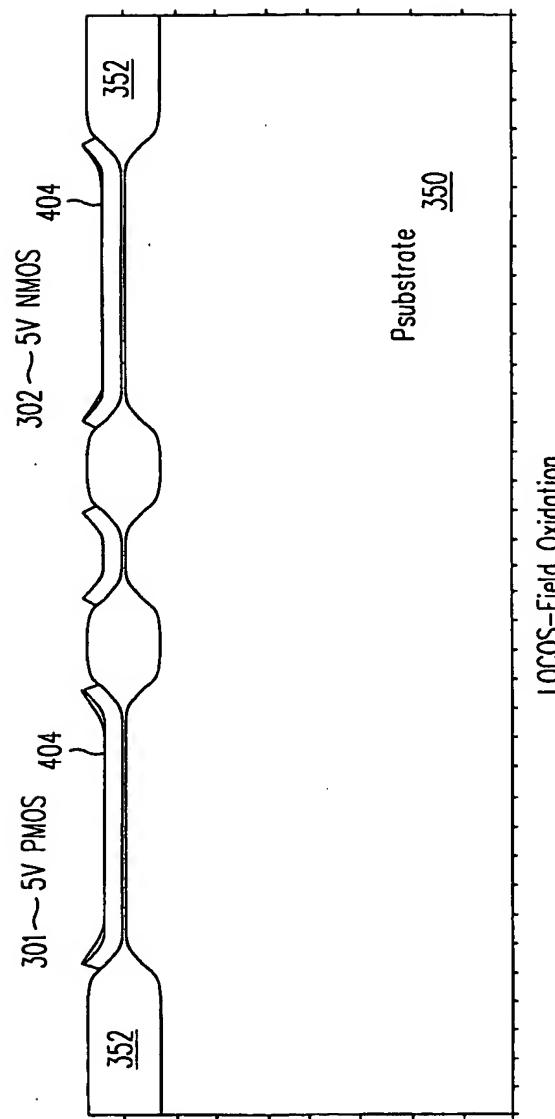
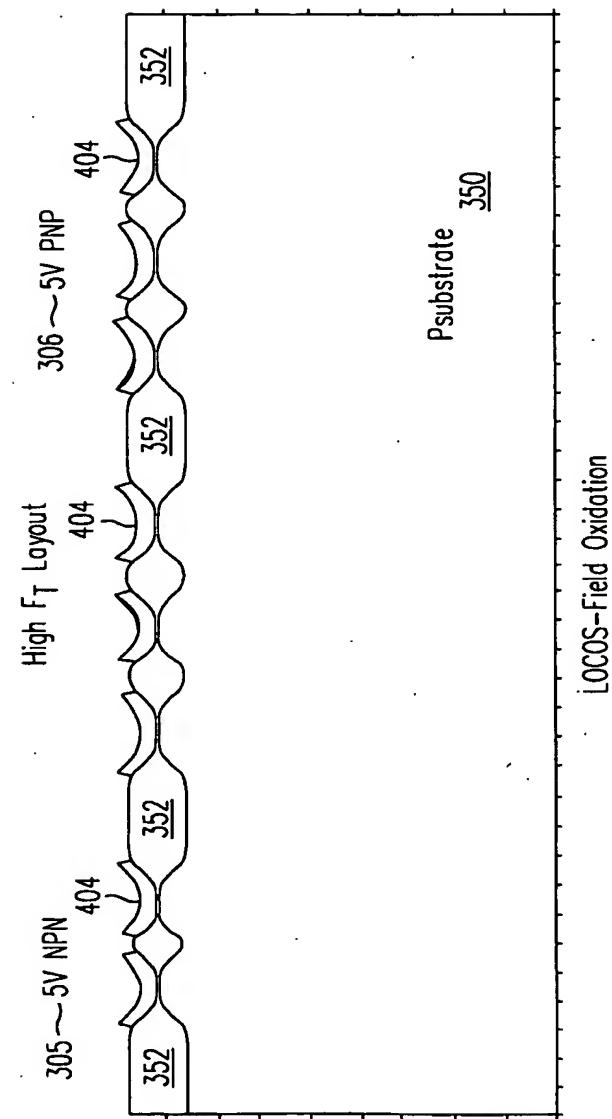


FIG. 23B



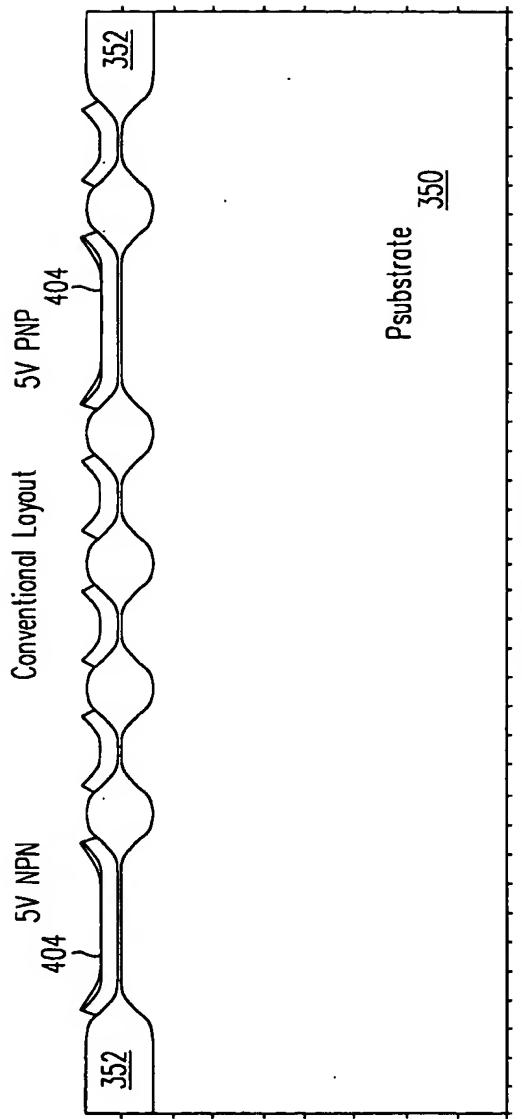


FIG. 23C

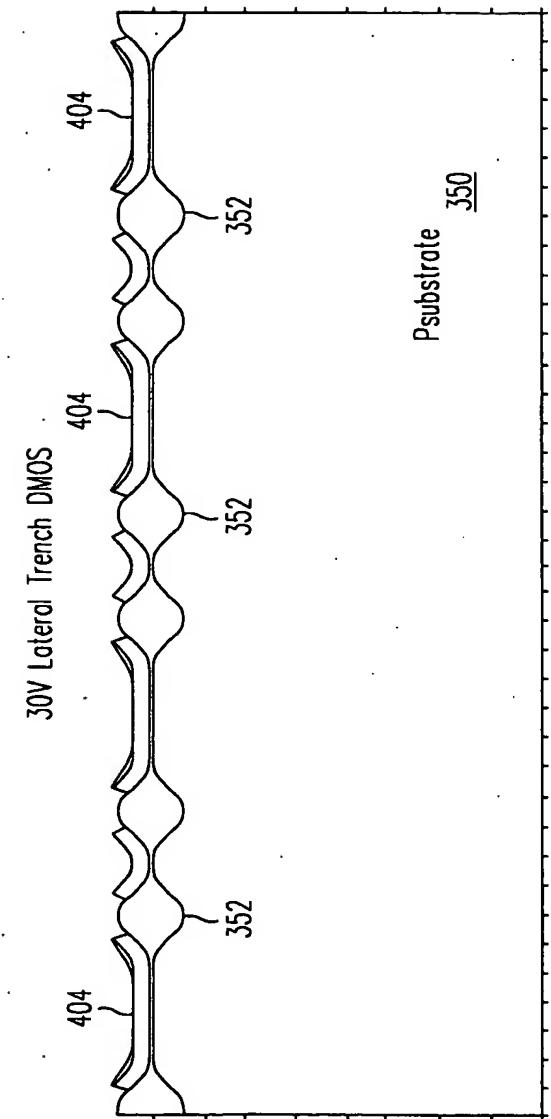


FIG. 23D

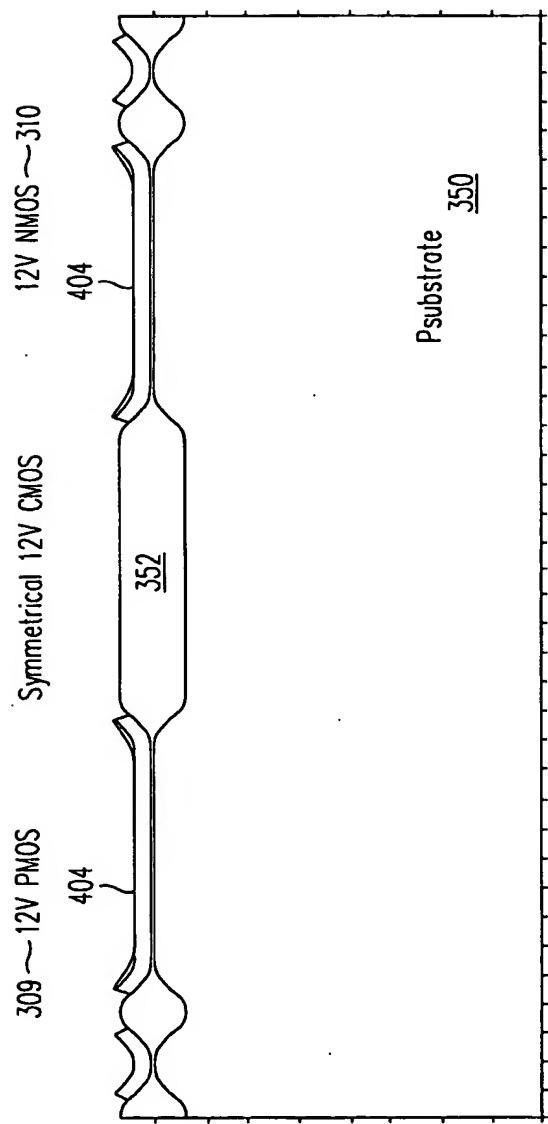


FIG. 23E

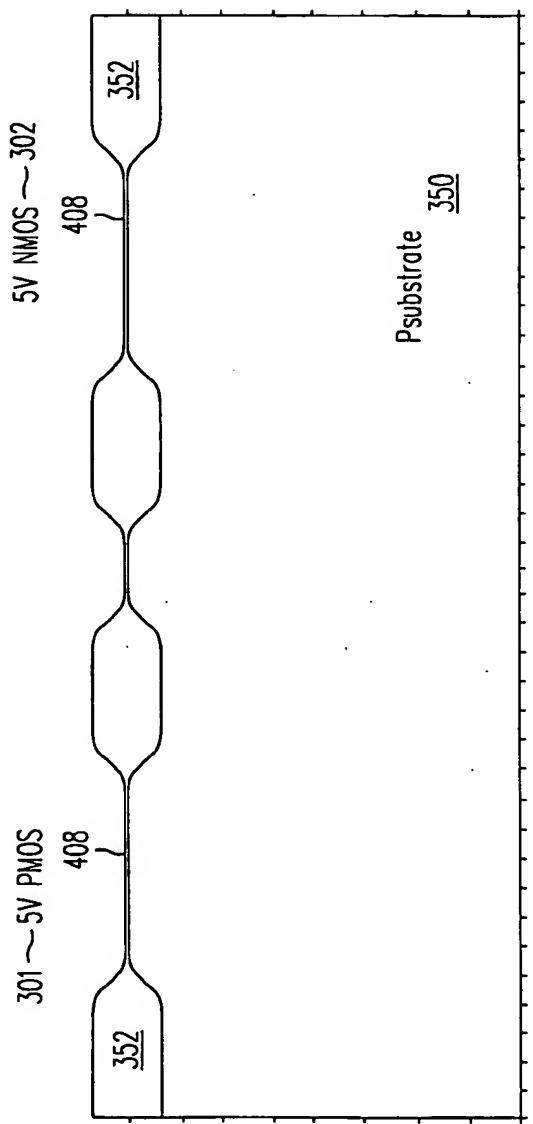


FIG. 24A

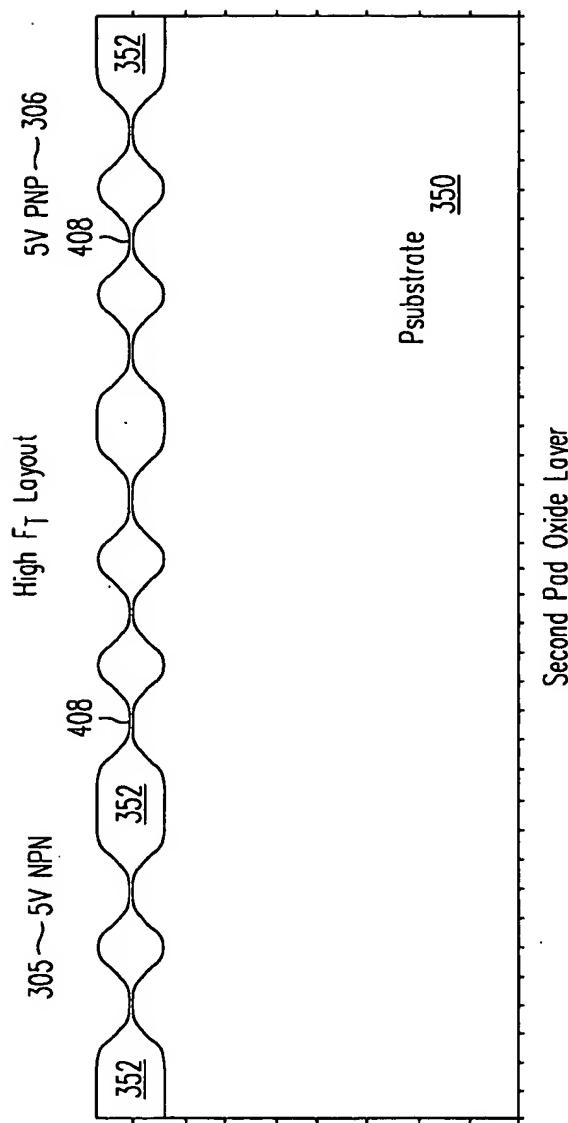


FIG. 24B

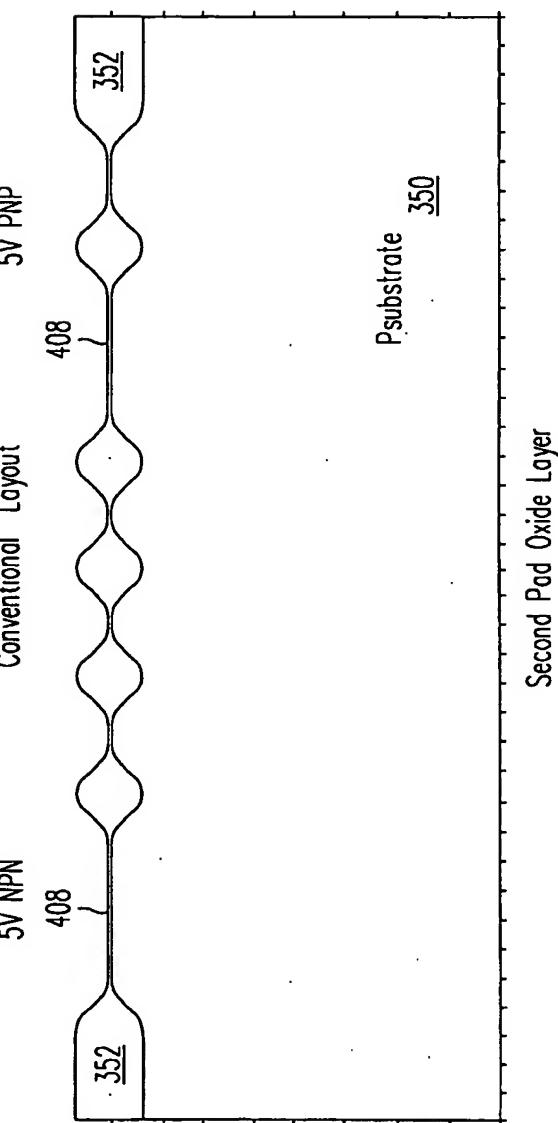


FIG. 24C

FIG. 24D

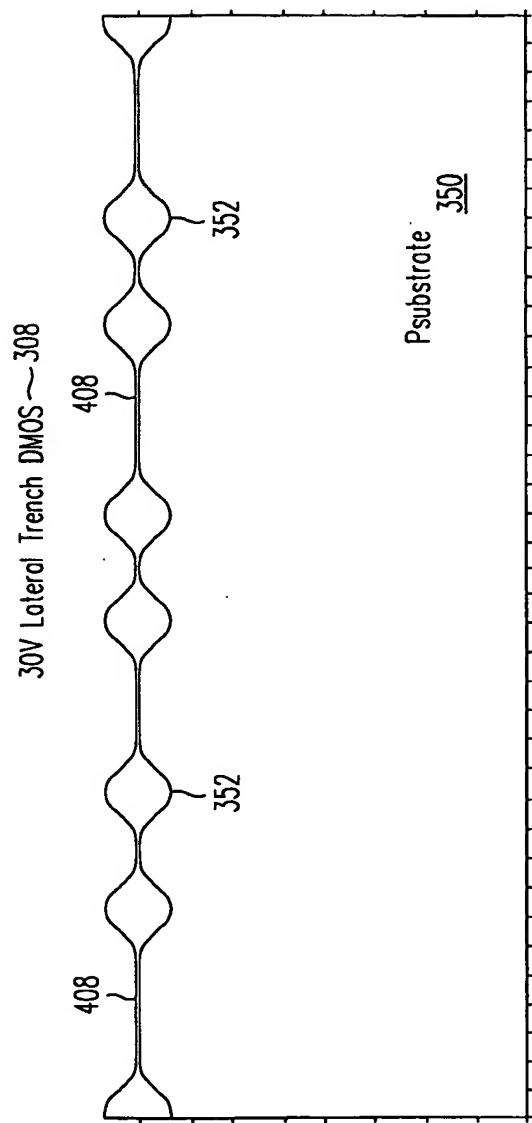
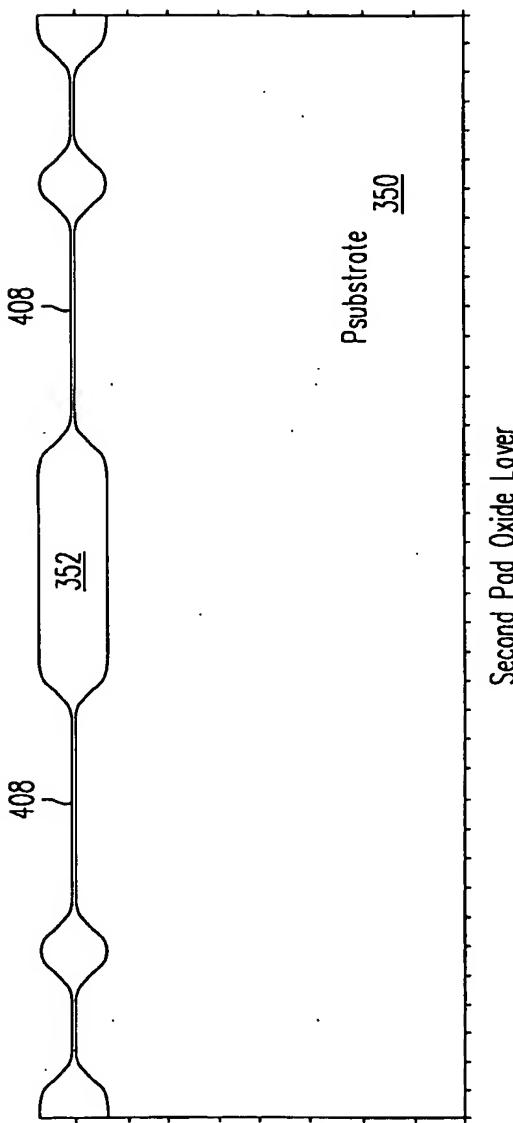


FIG. 24E



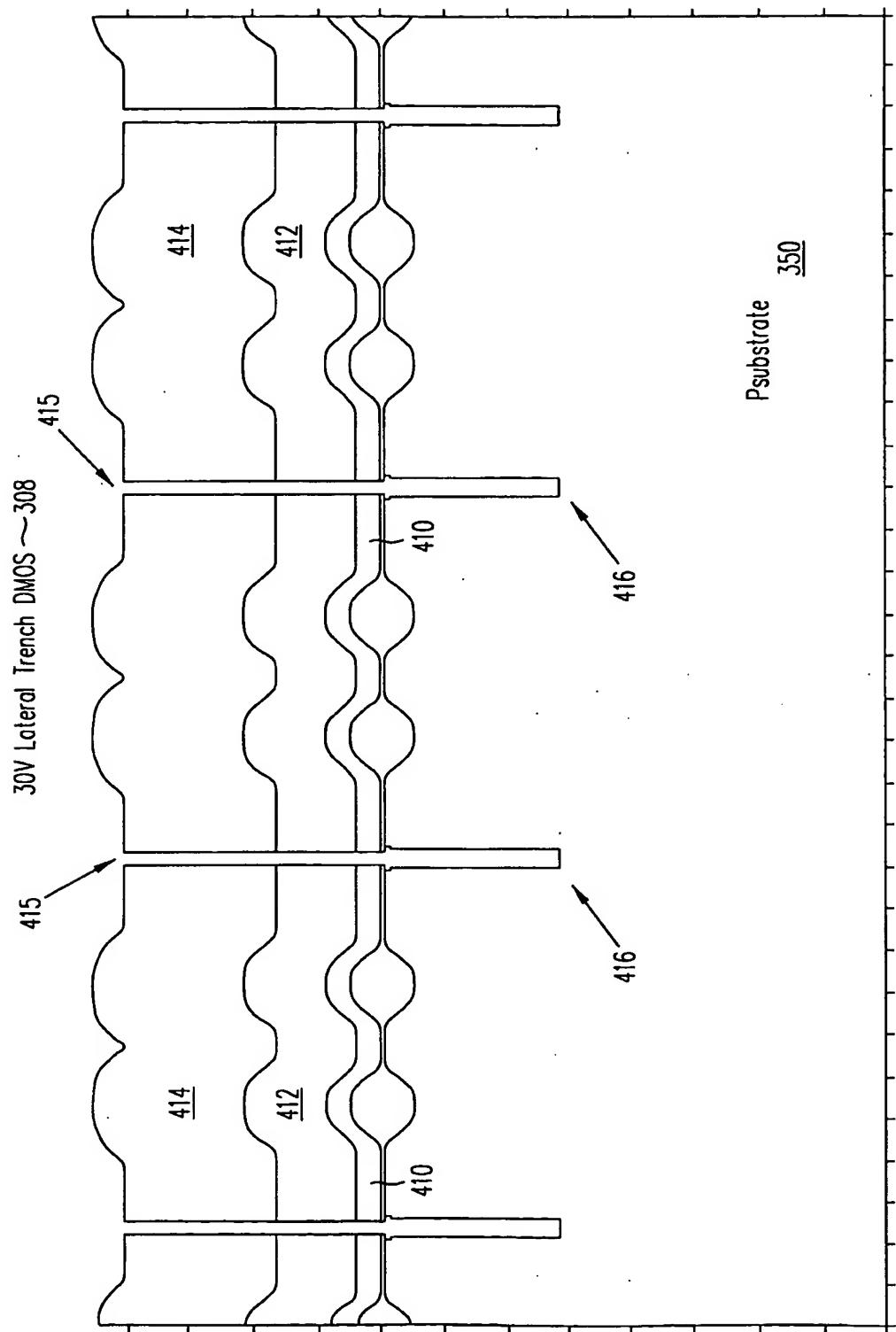
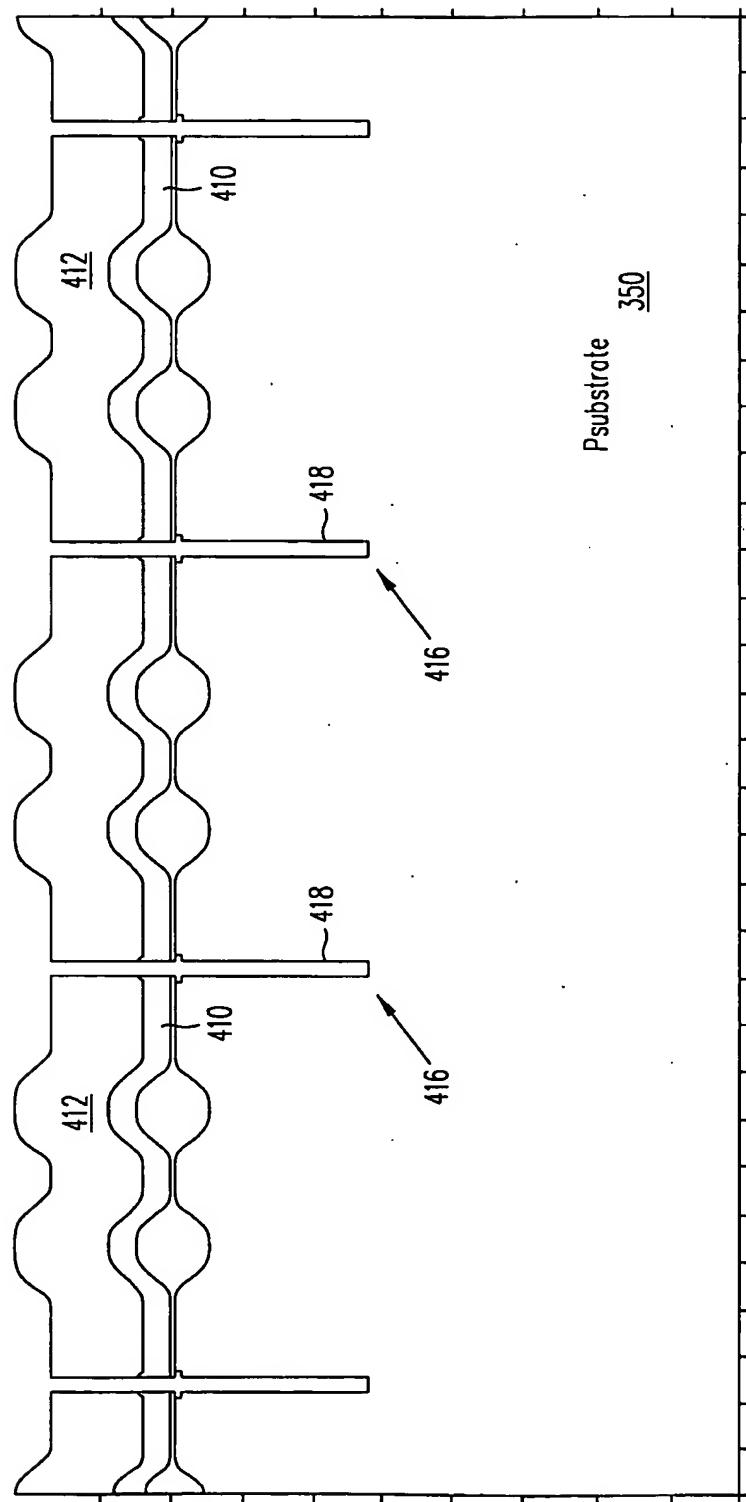


FIG. 25D

30V Lateral Trench DMOS ~308



Sacrificial Oxide

FIG. 26D

30V Lateral Trench DMOS ~308

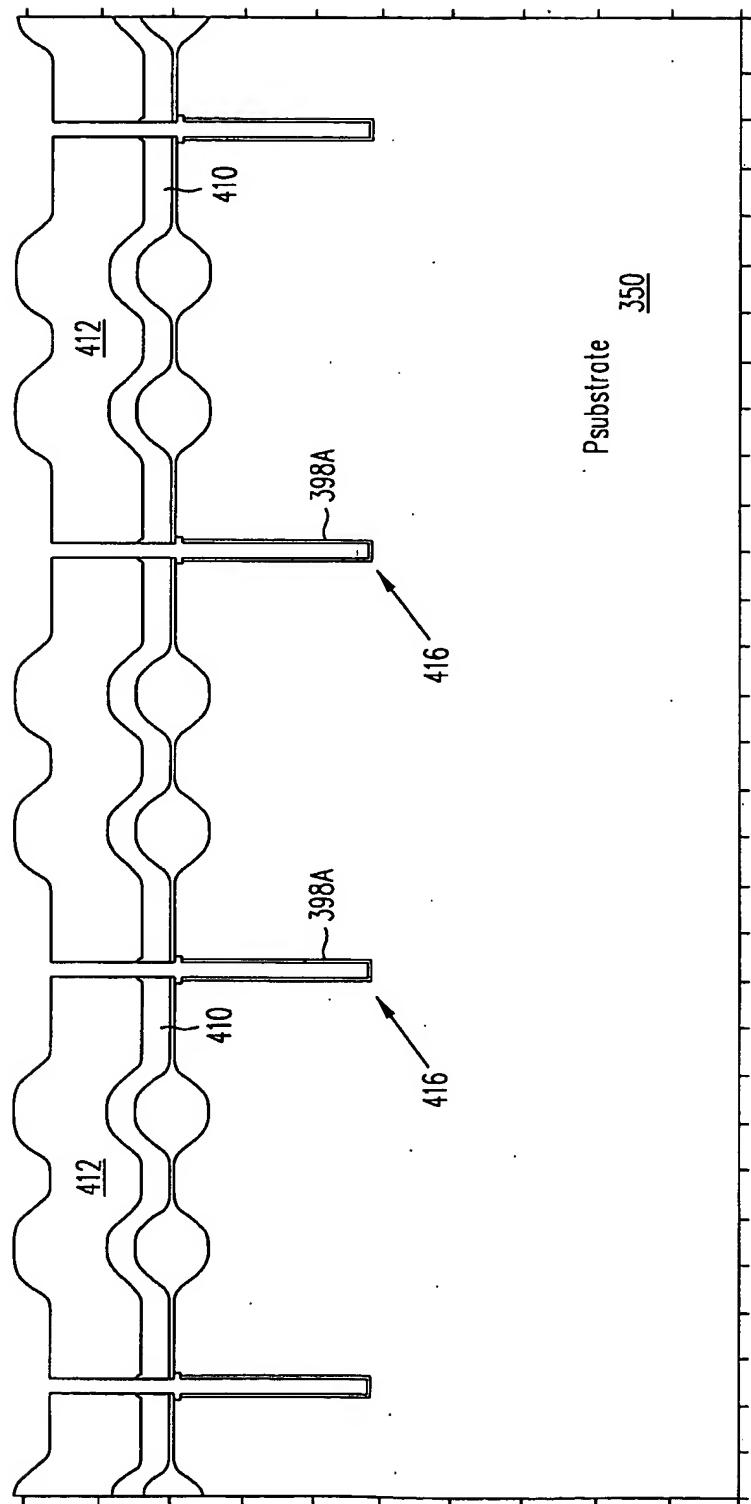
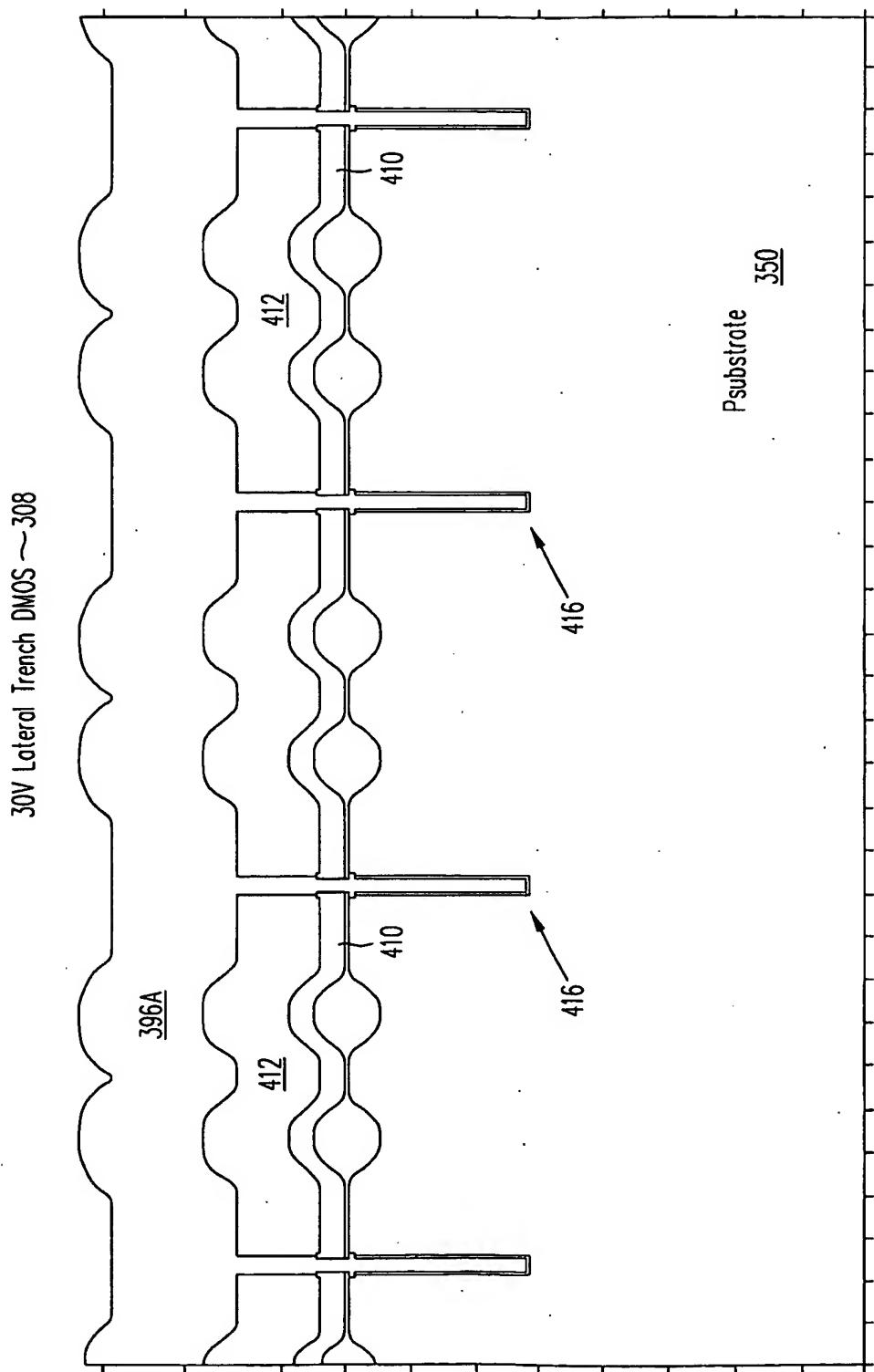
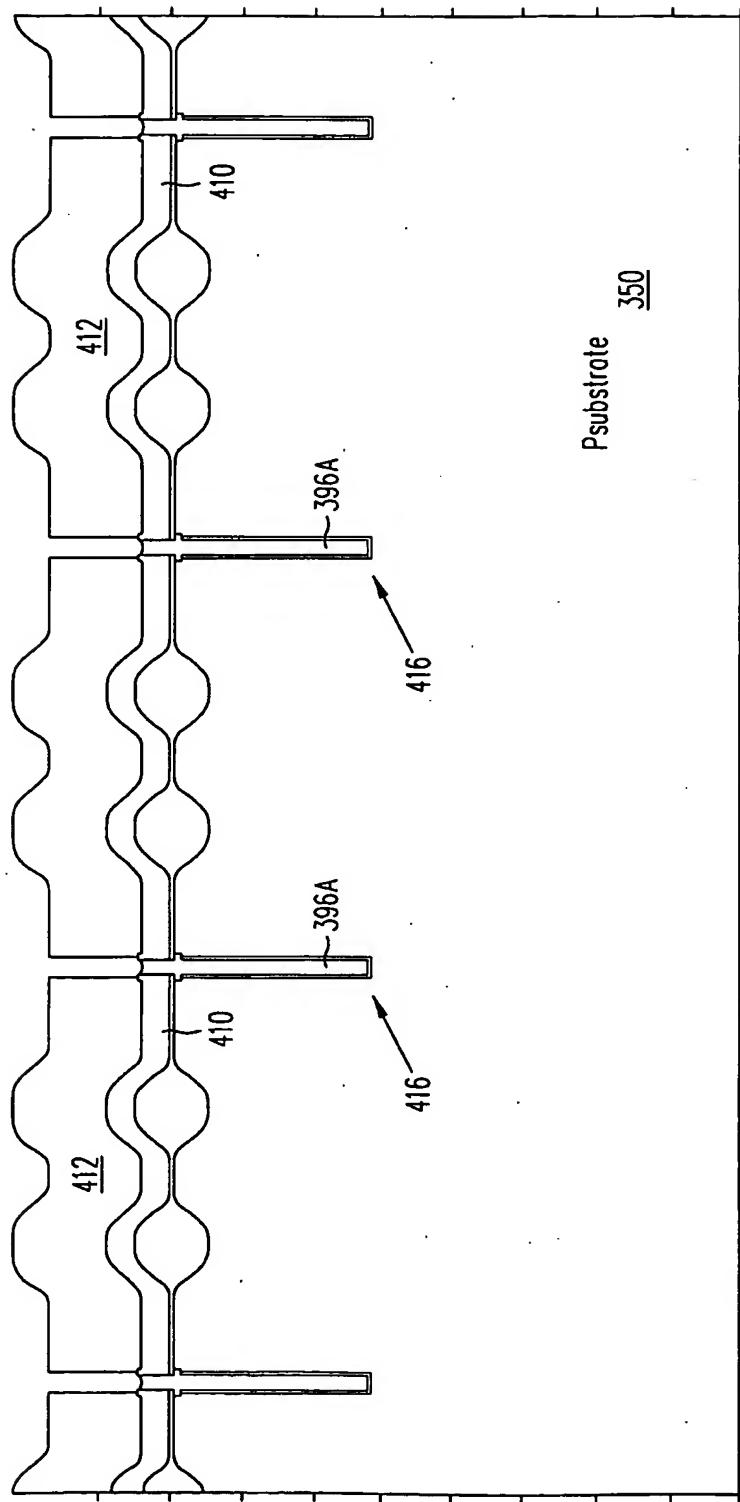


FIG. 27D

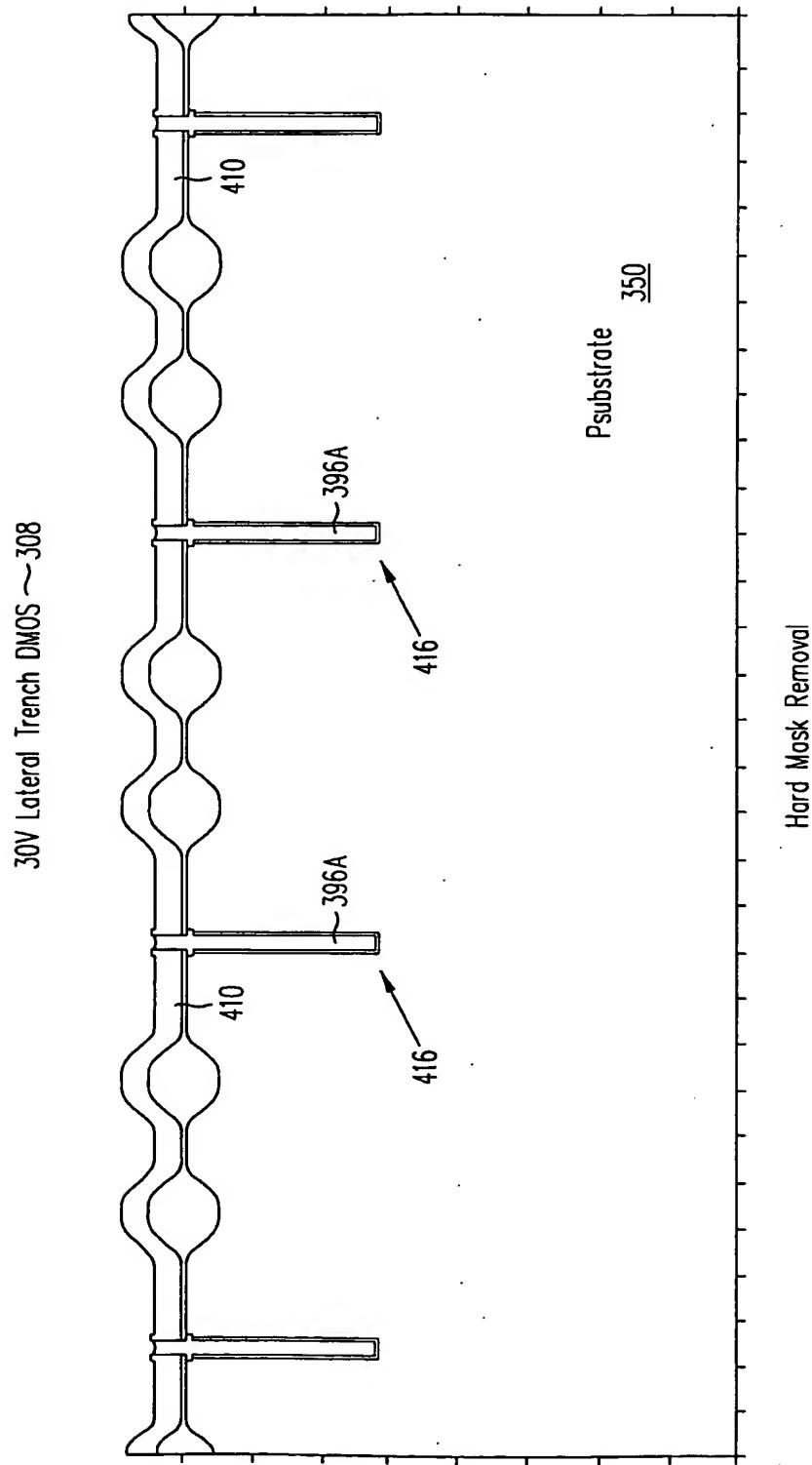


30V Lateral Trench DMOS ~308



Poly-silicon Etchback-First Layer

FIG. 29D



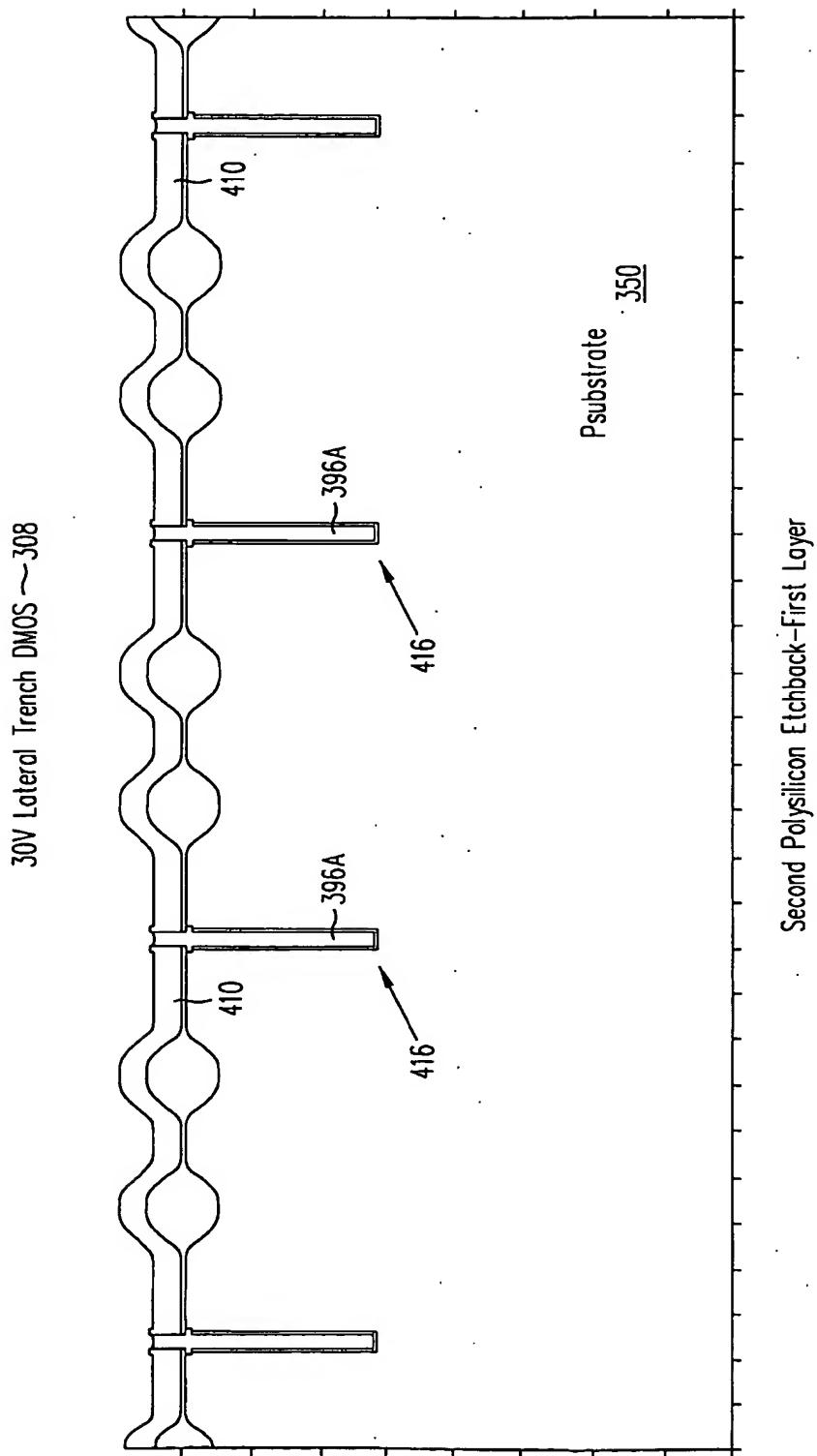


FIG. 31D

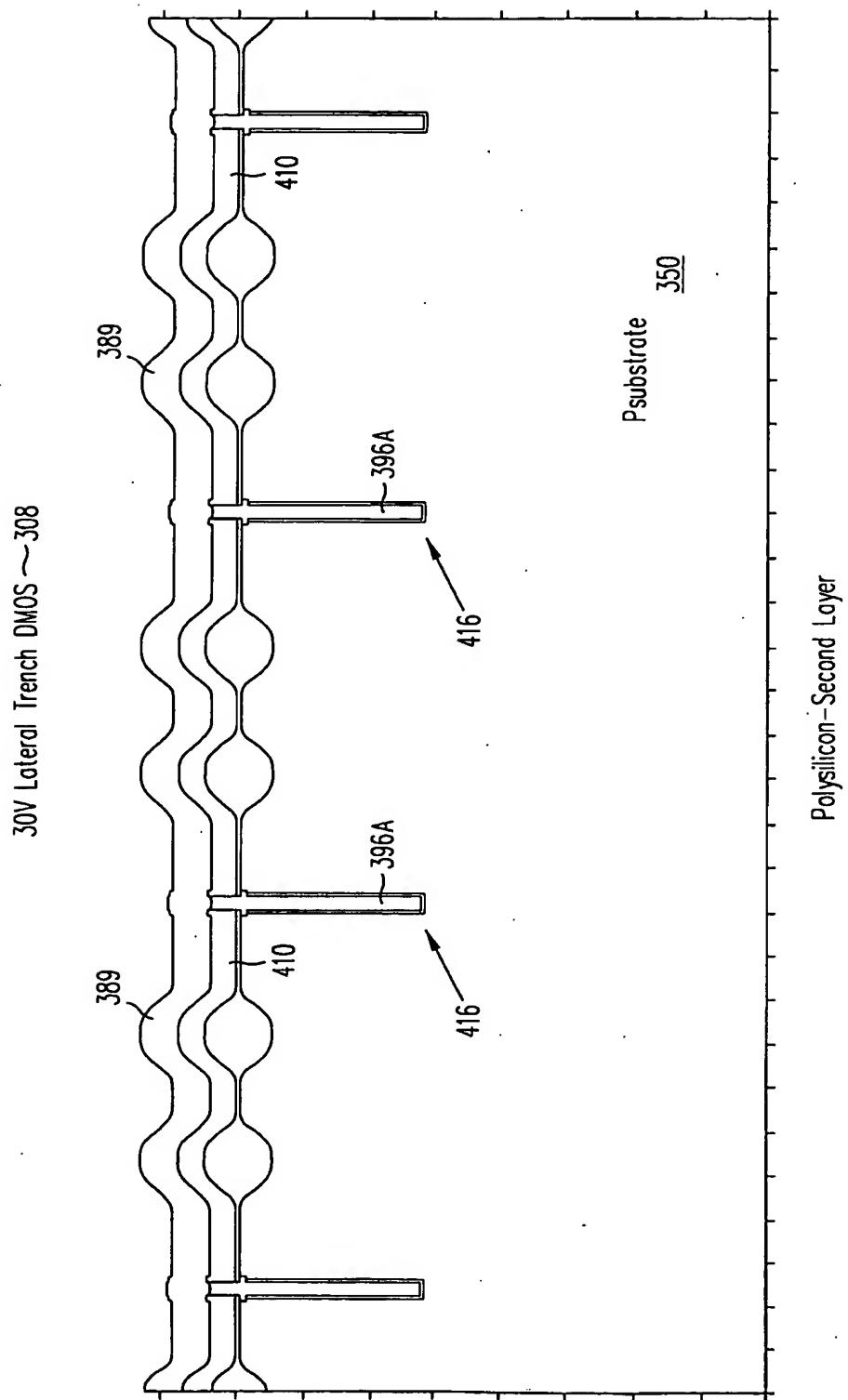
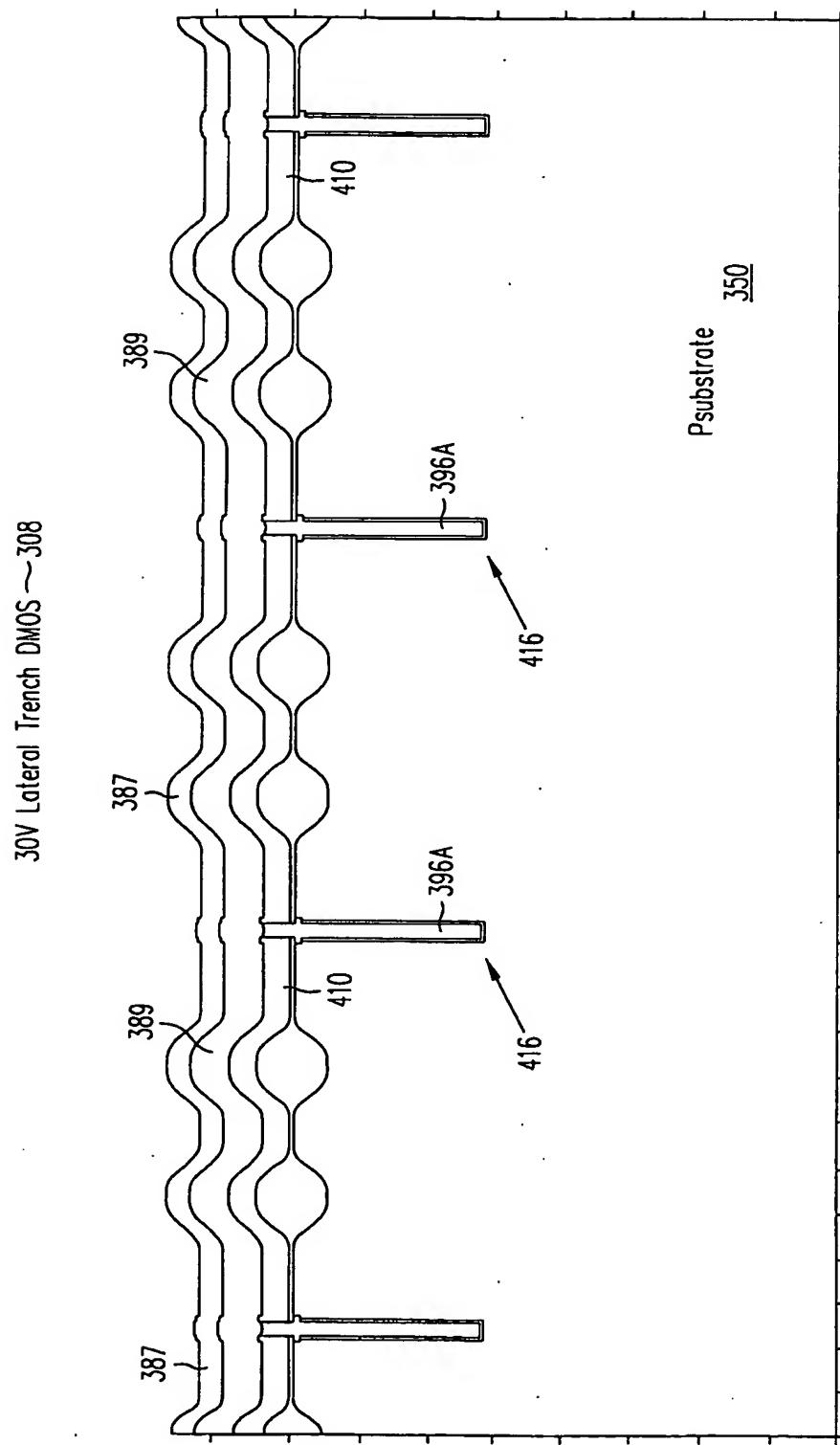


FIG. 32D



Interlayer Dielectric

FIG. 33D

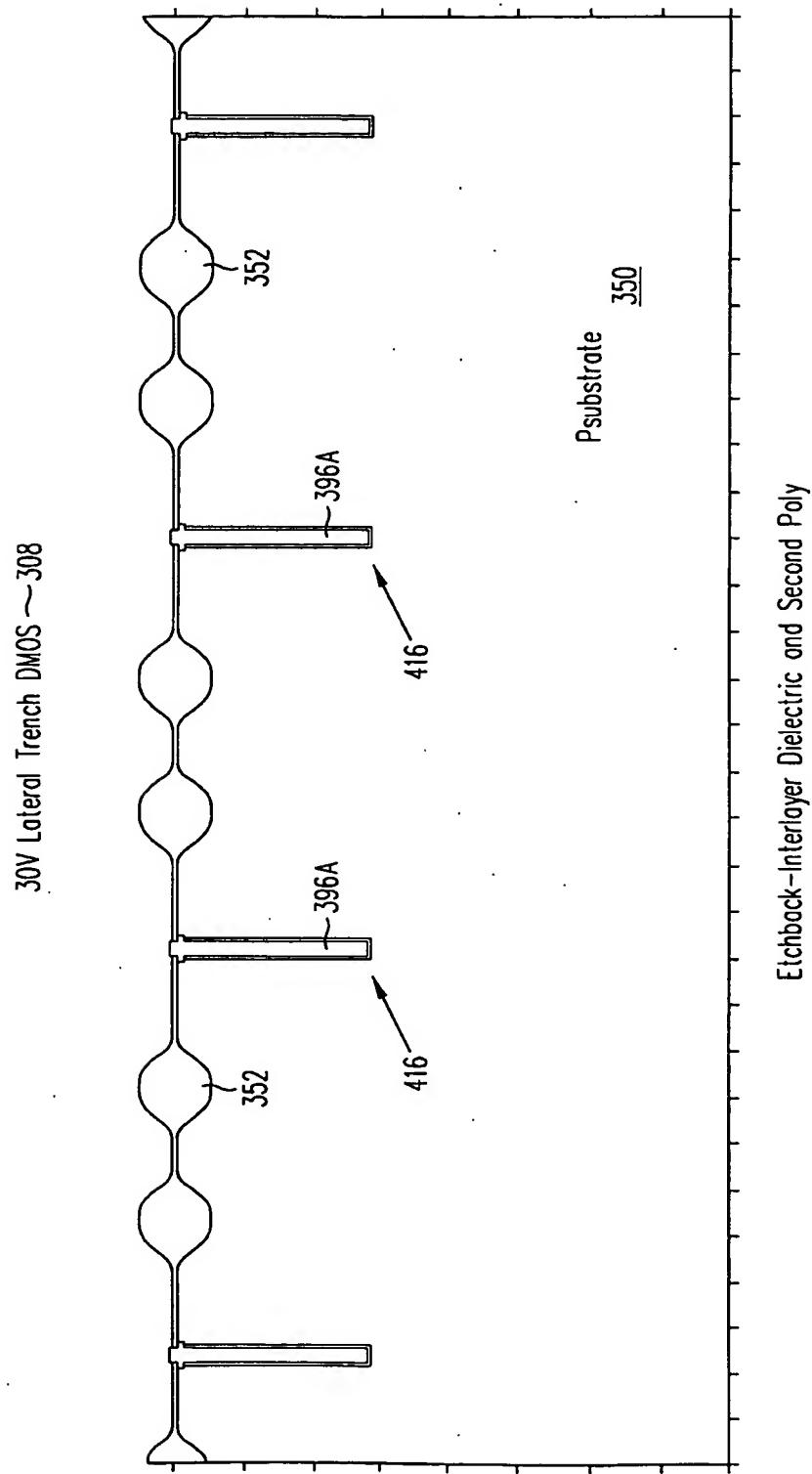


FIG. 34D

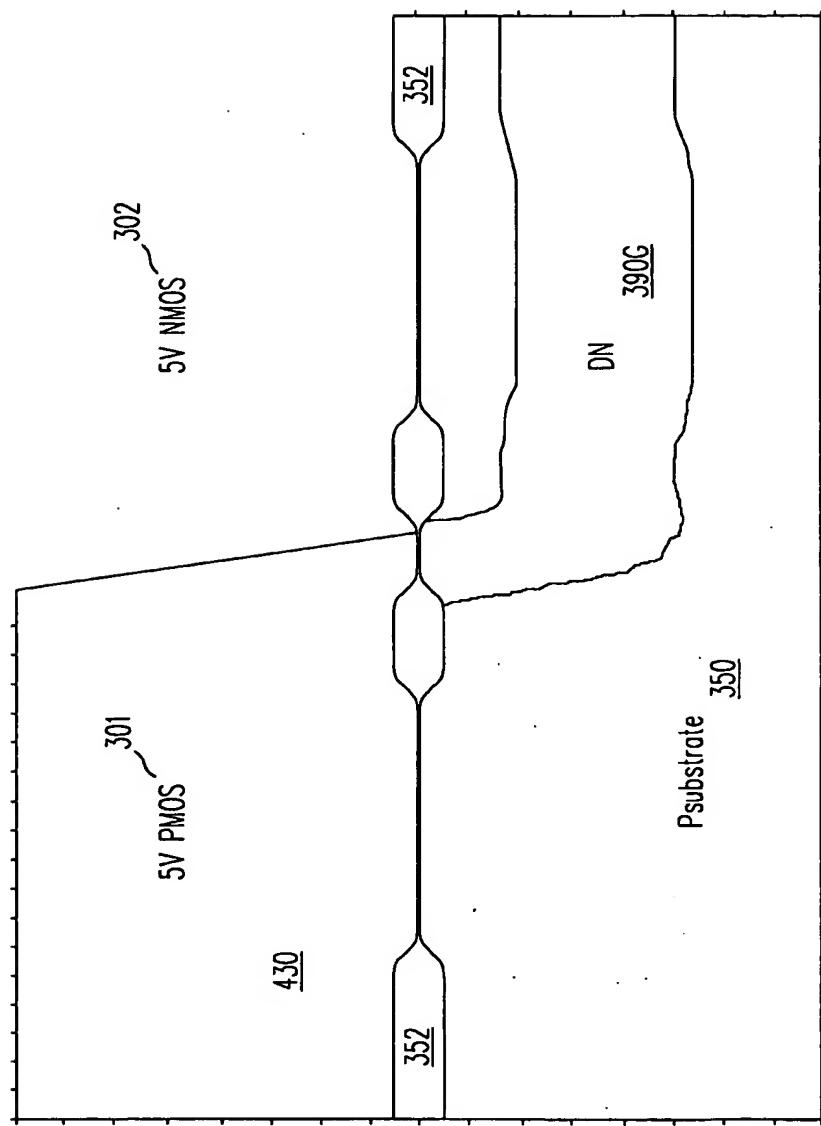
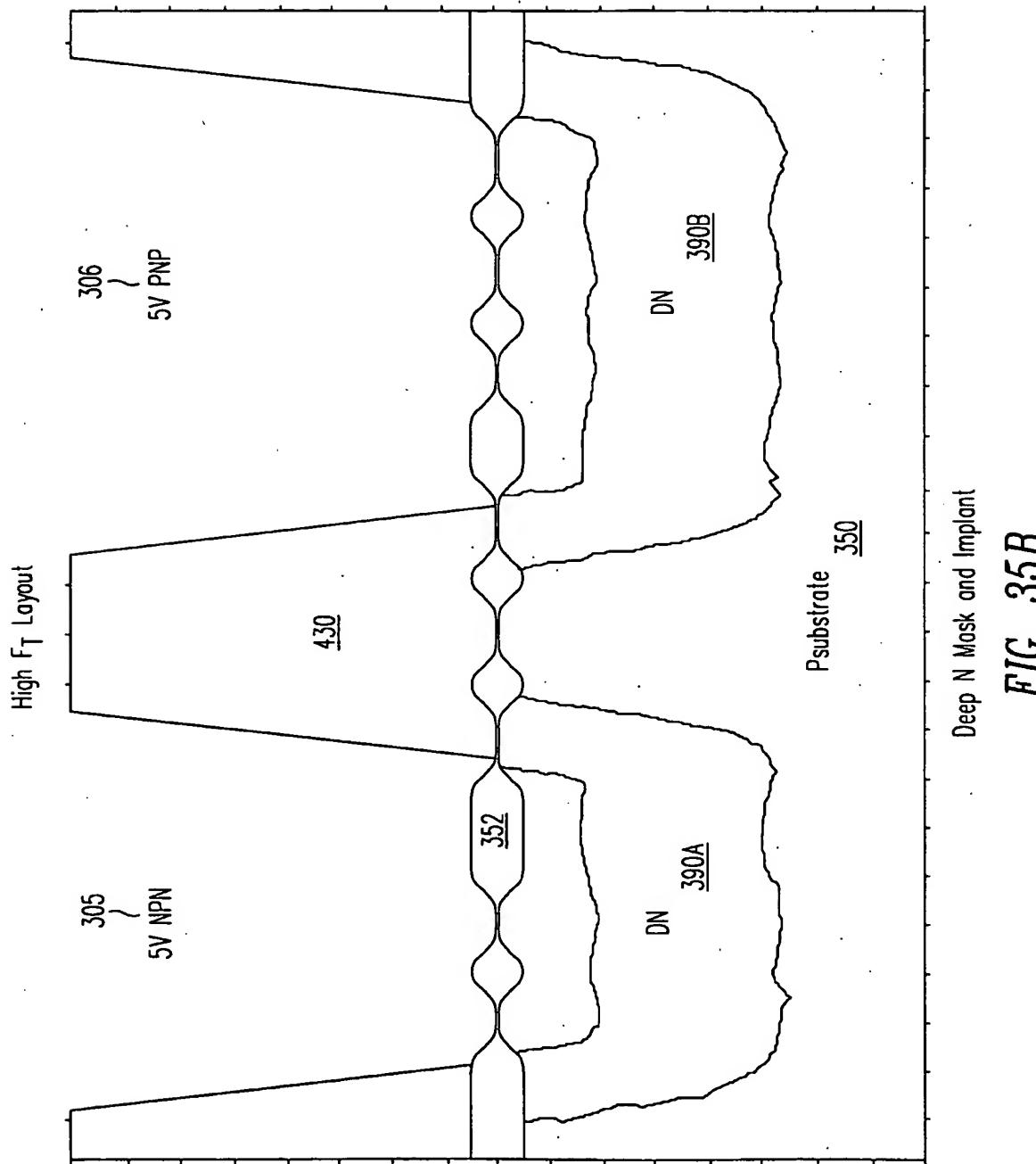
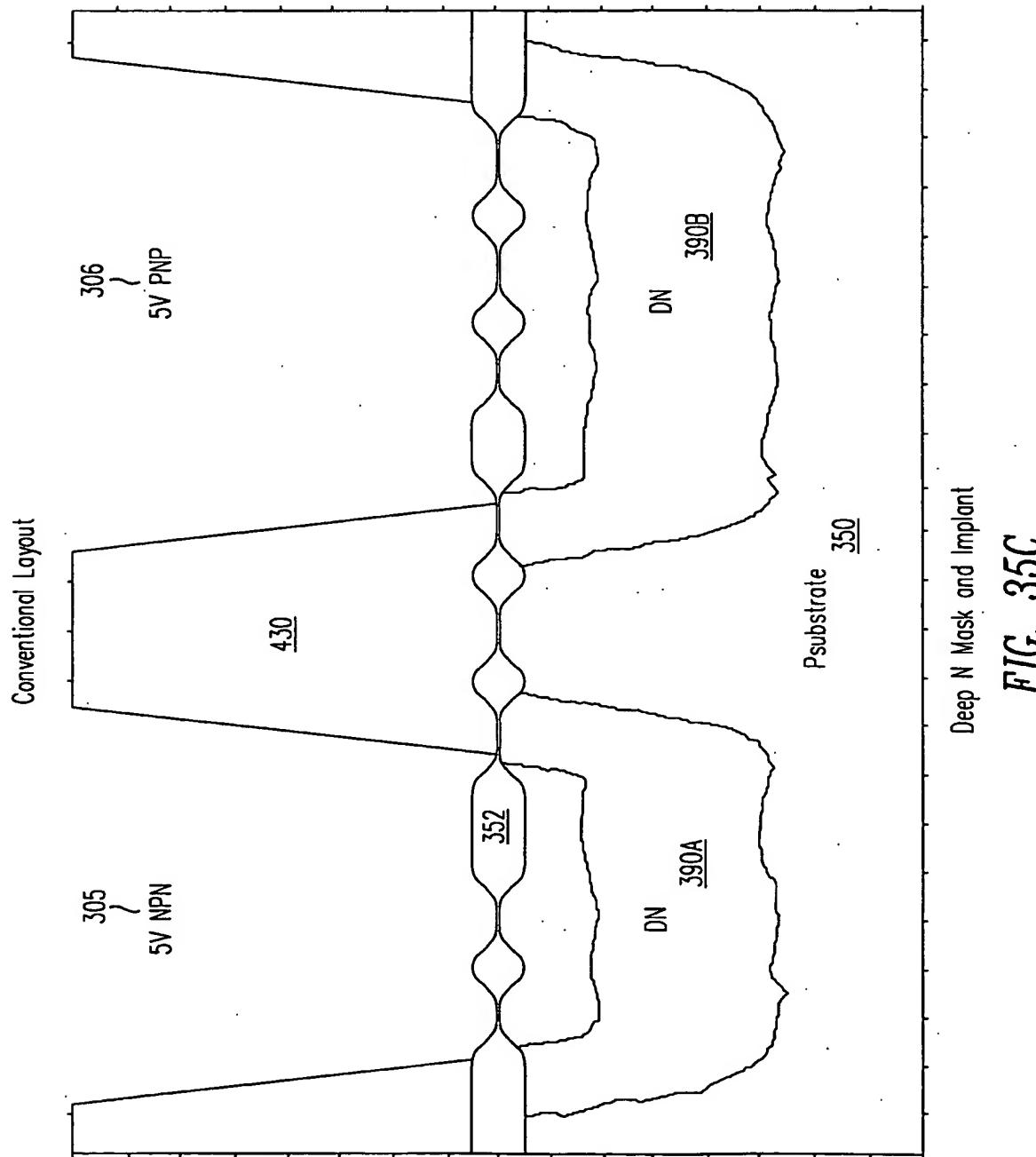


FIG. 35A

Deep N Mask and implant





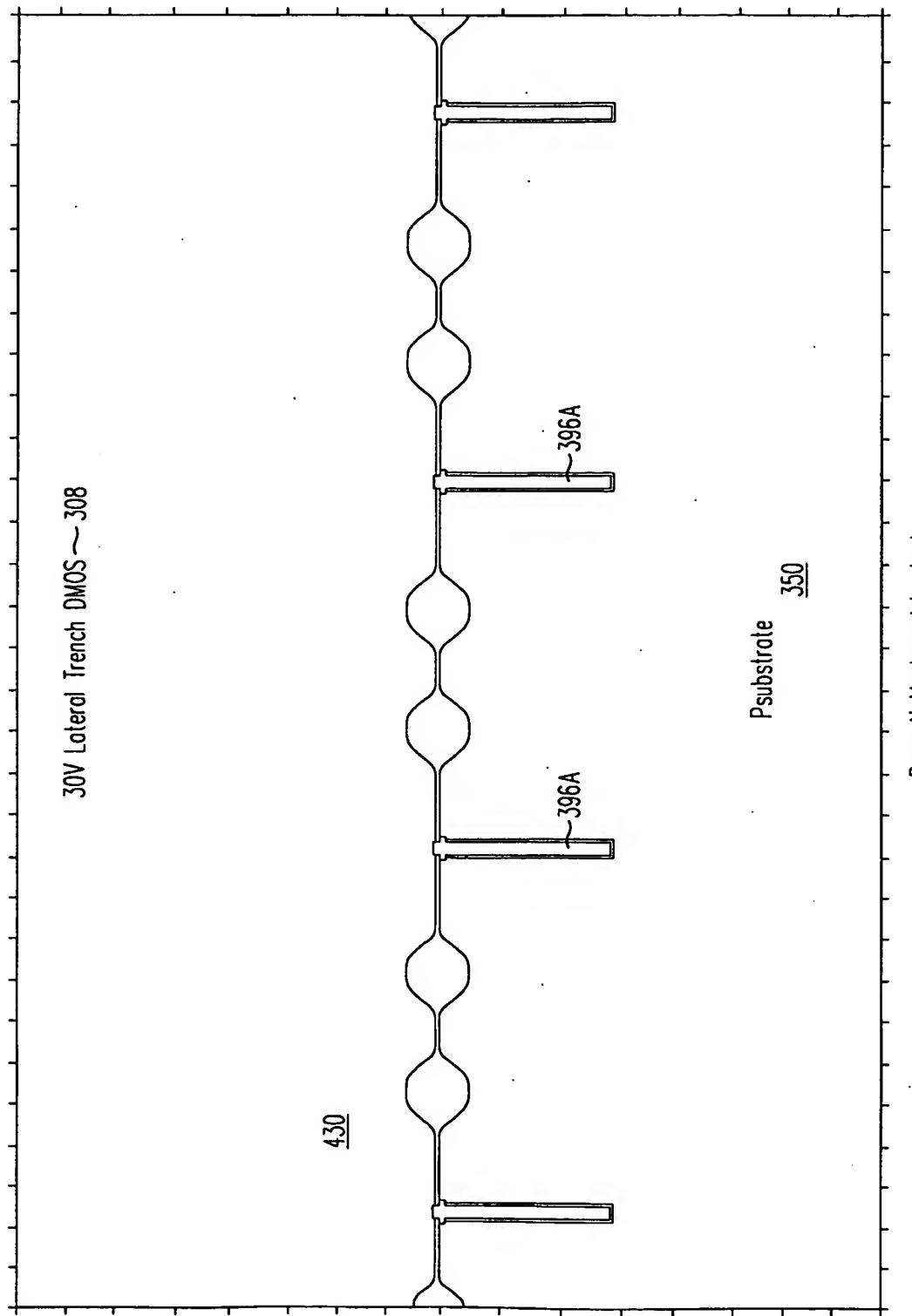


FIG. 35D

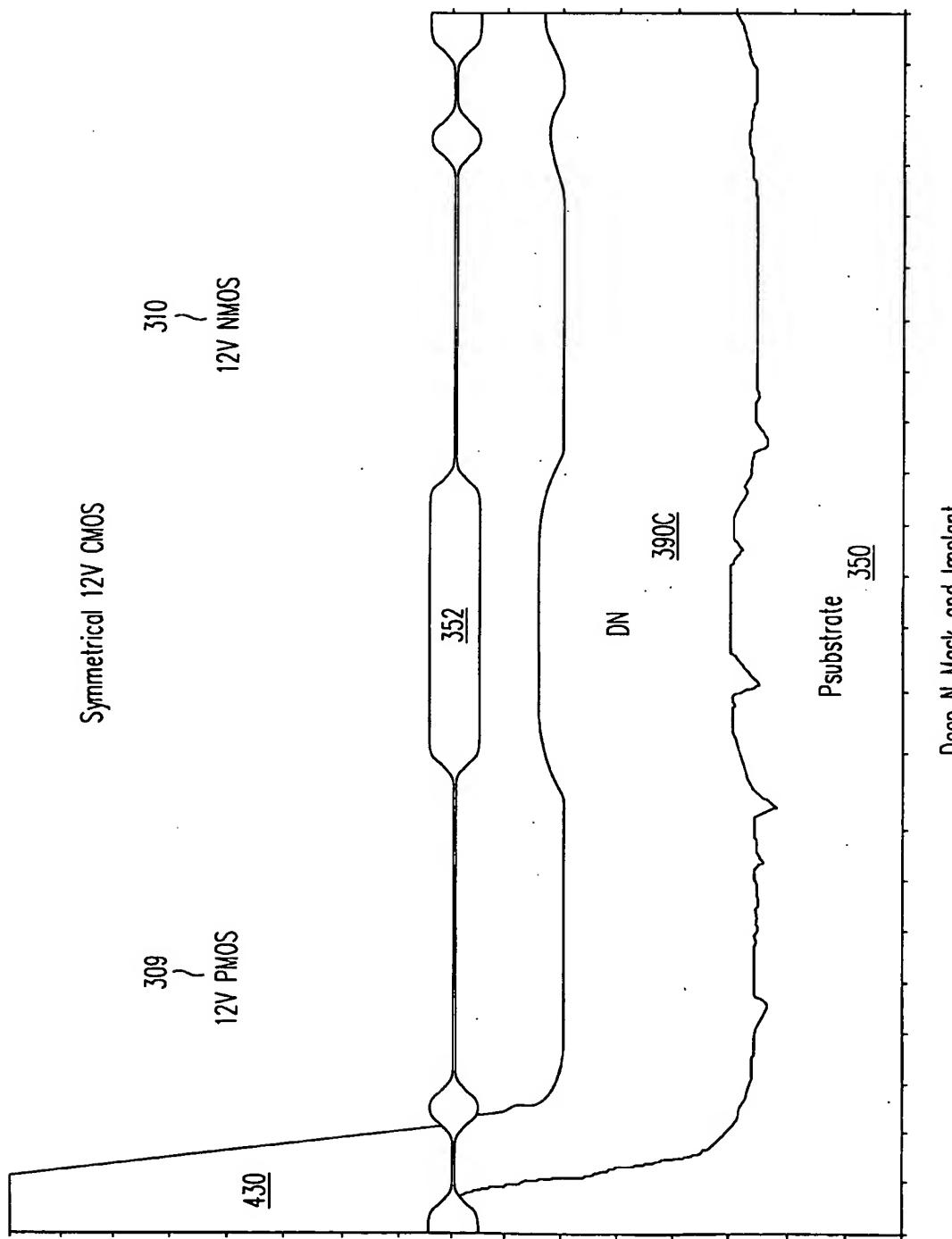


FIG. 35E

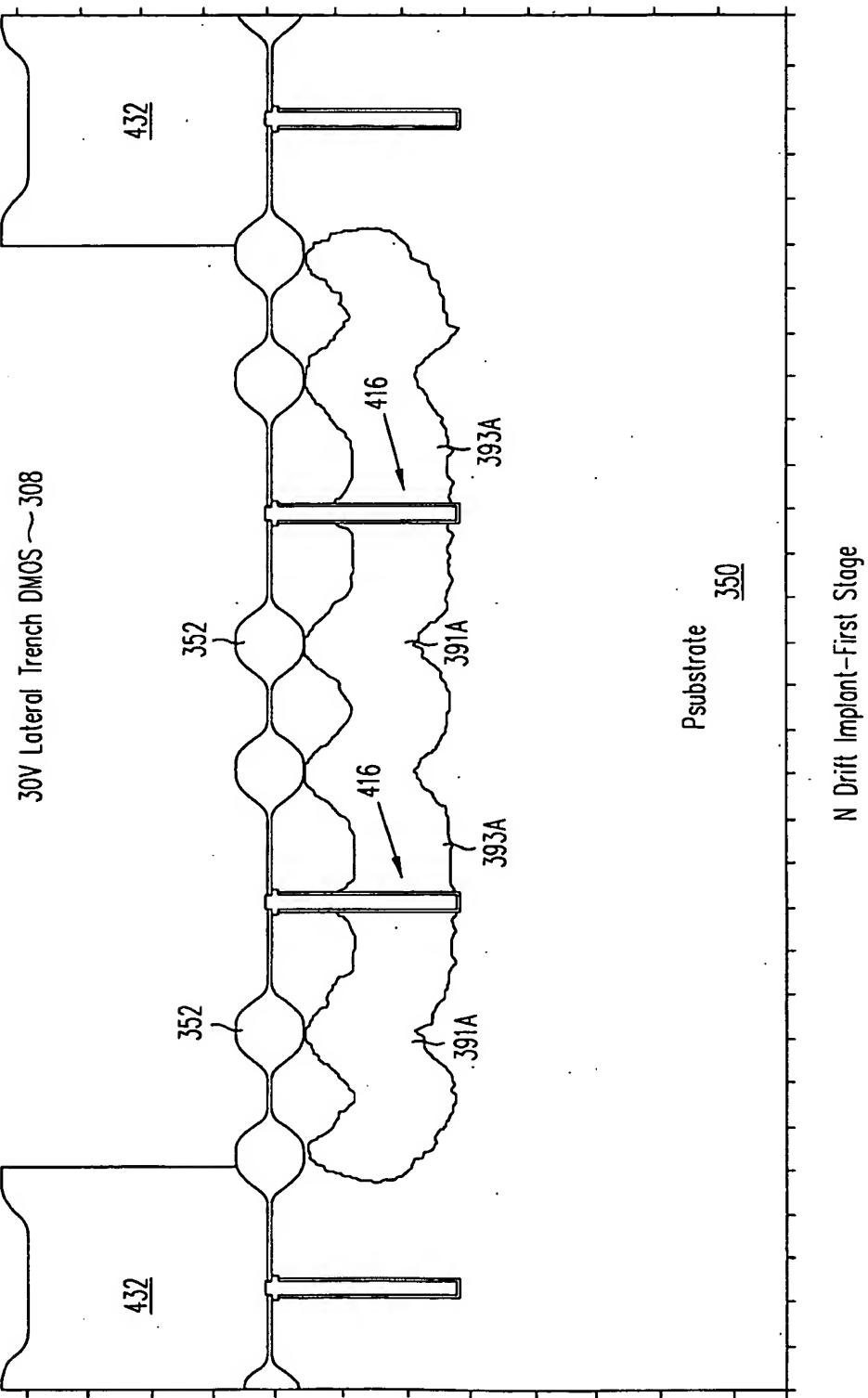
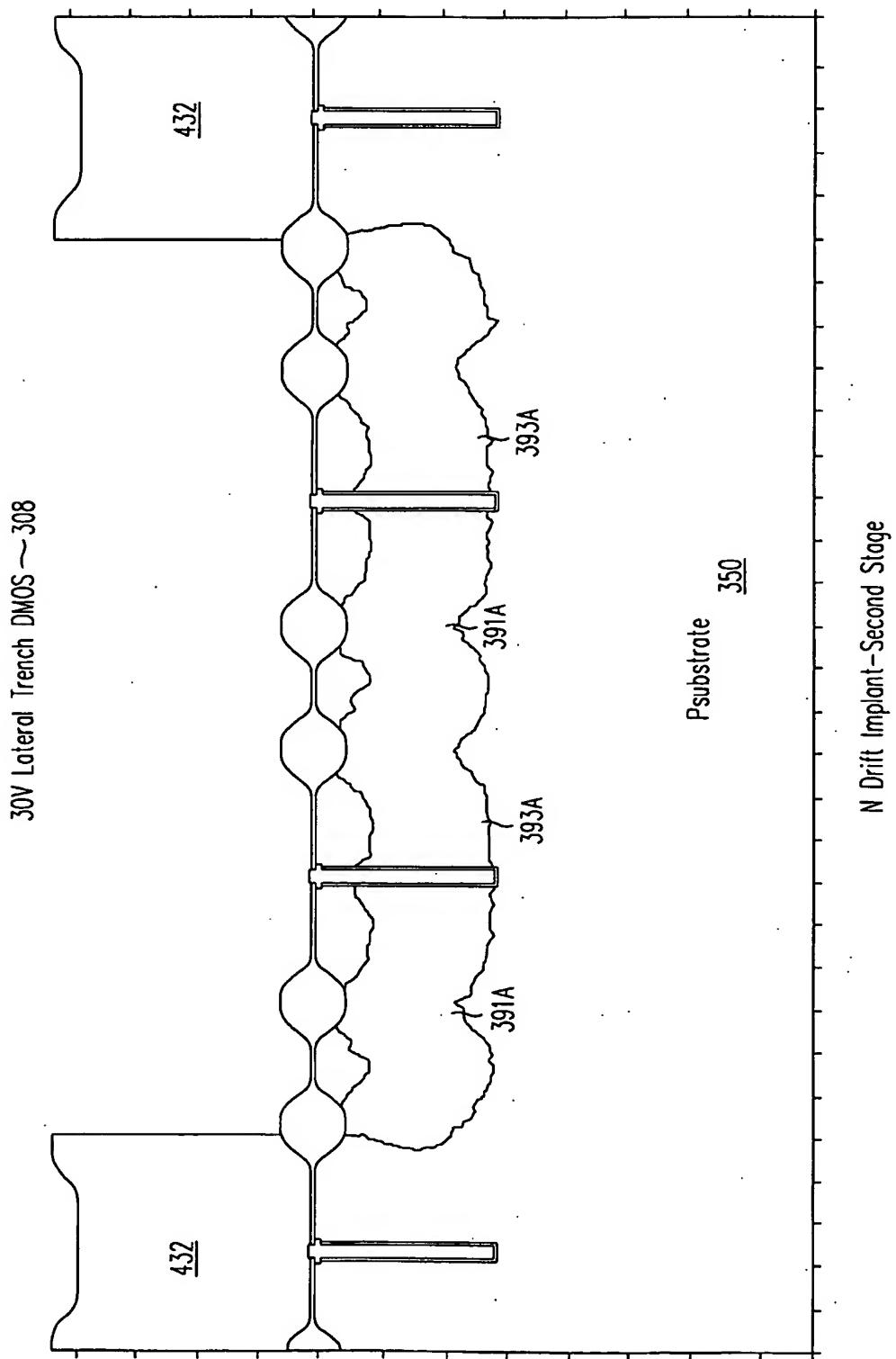
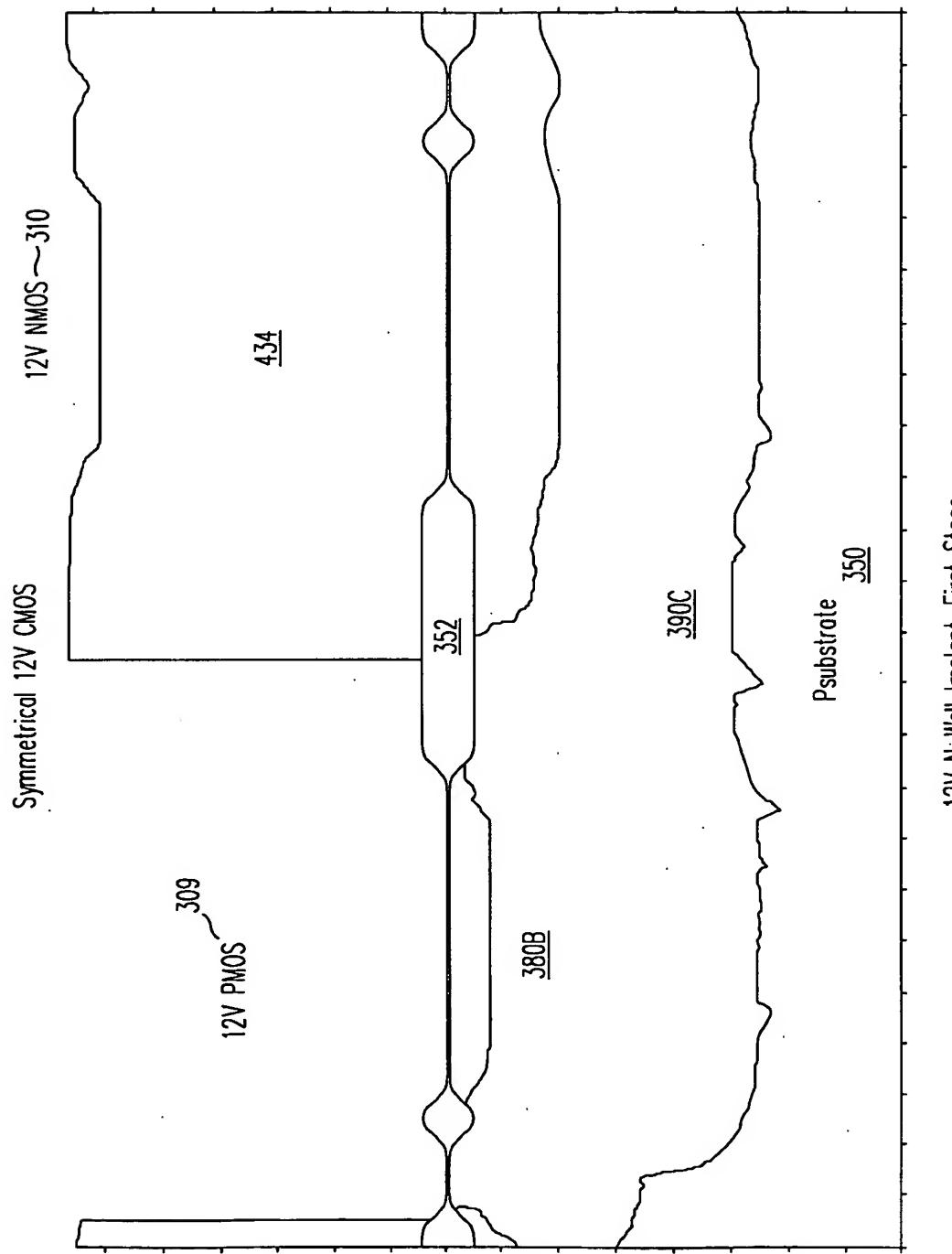


FIG. 36D





12V N Well Implant-First Stage

FIG. 38E

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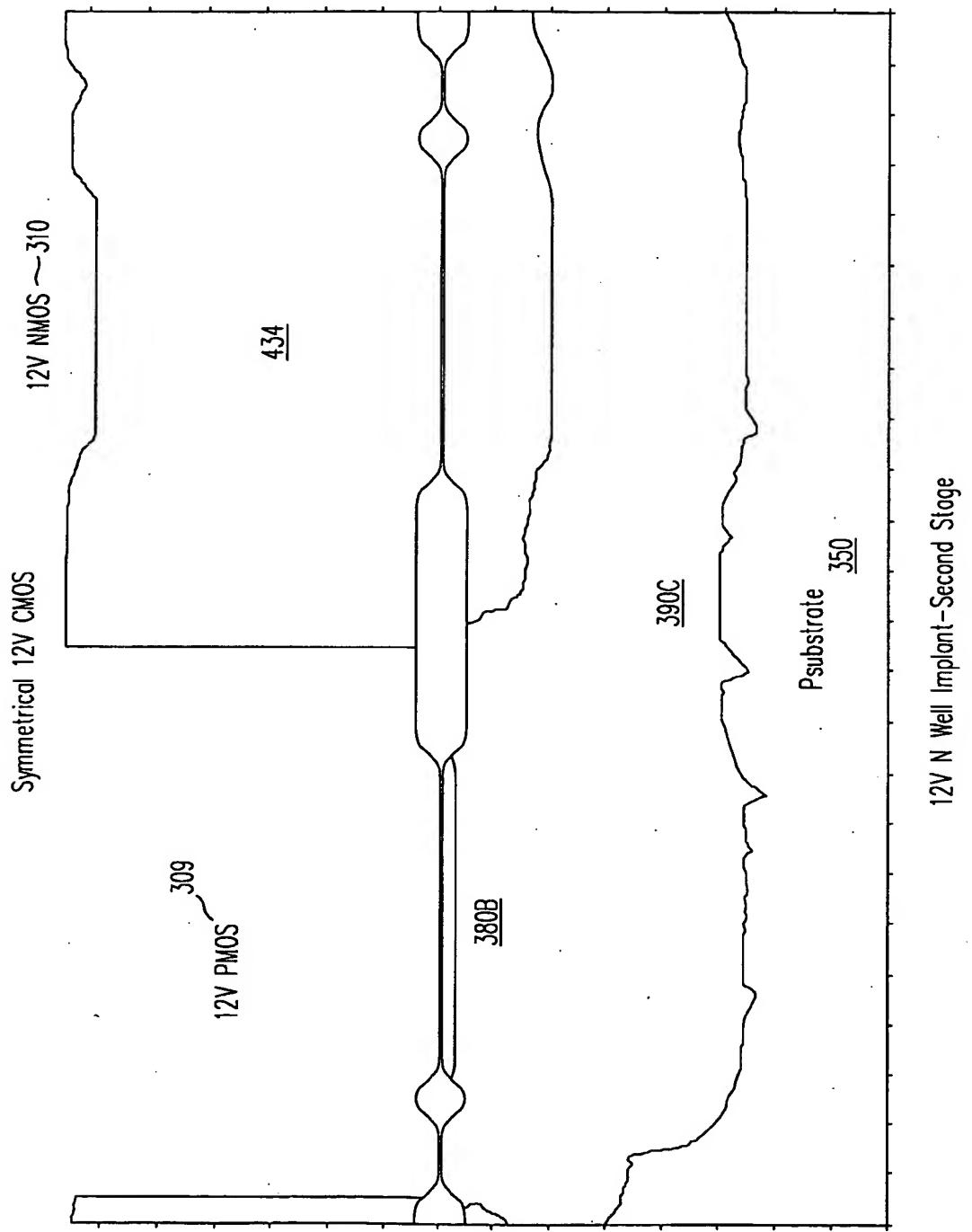
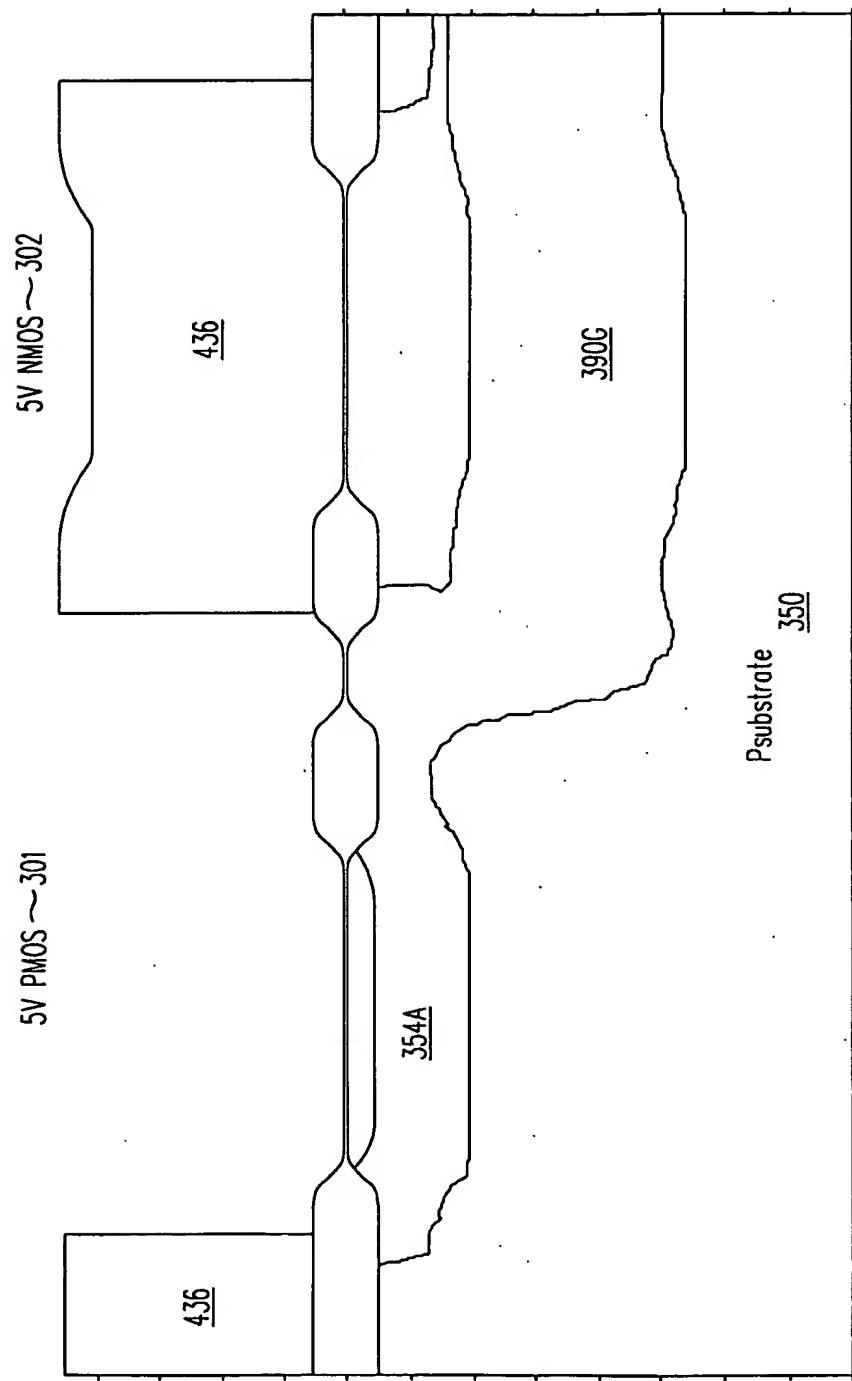
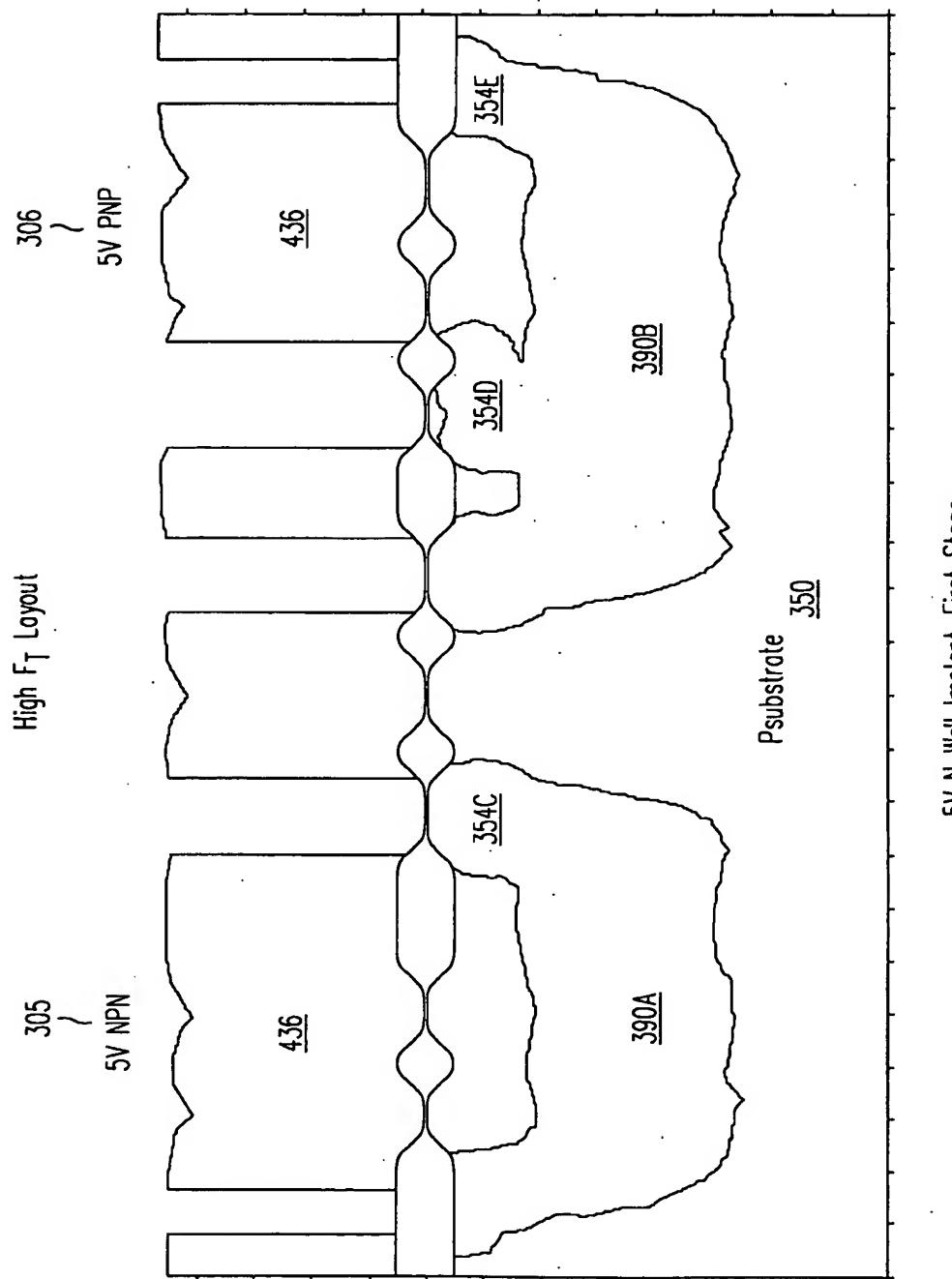


FIG. 39E



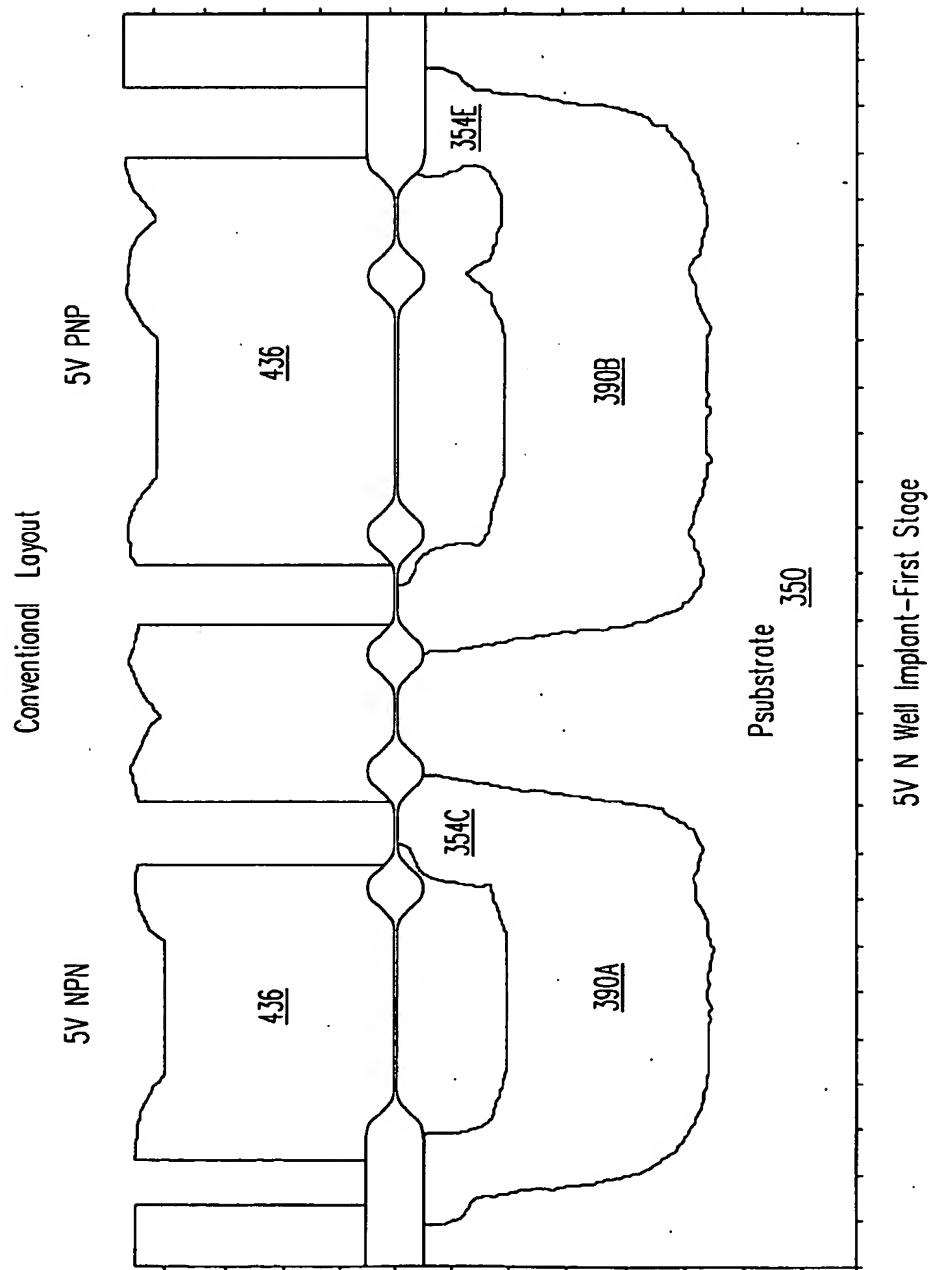
5V N Well Implant - First Stage

FIG. 40A



5V N Well Implant-First Stage

FIG. 40B



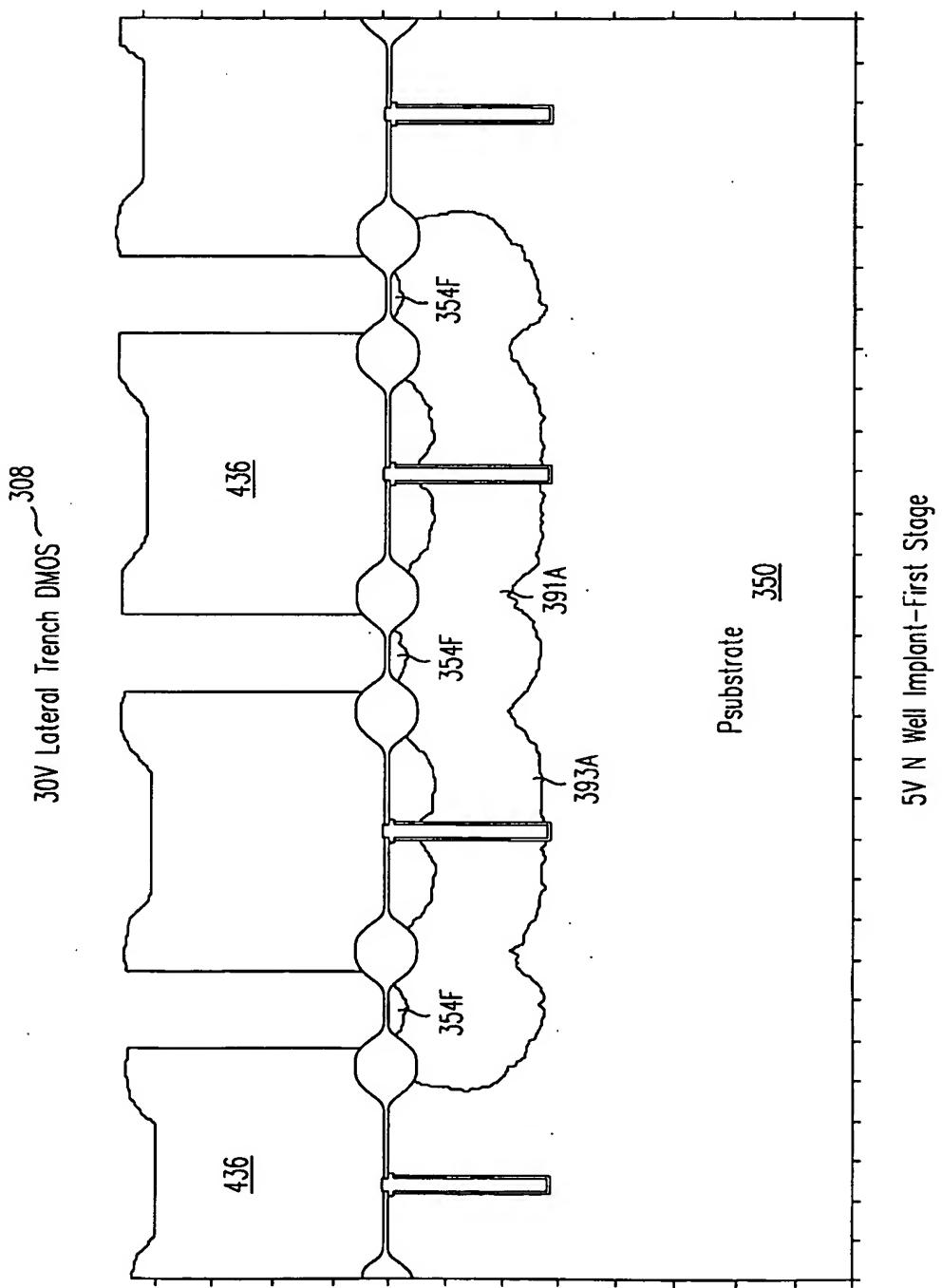
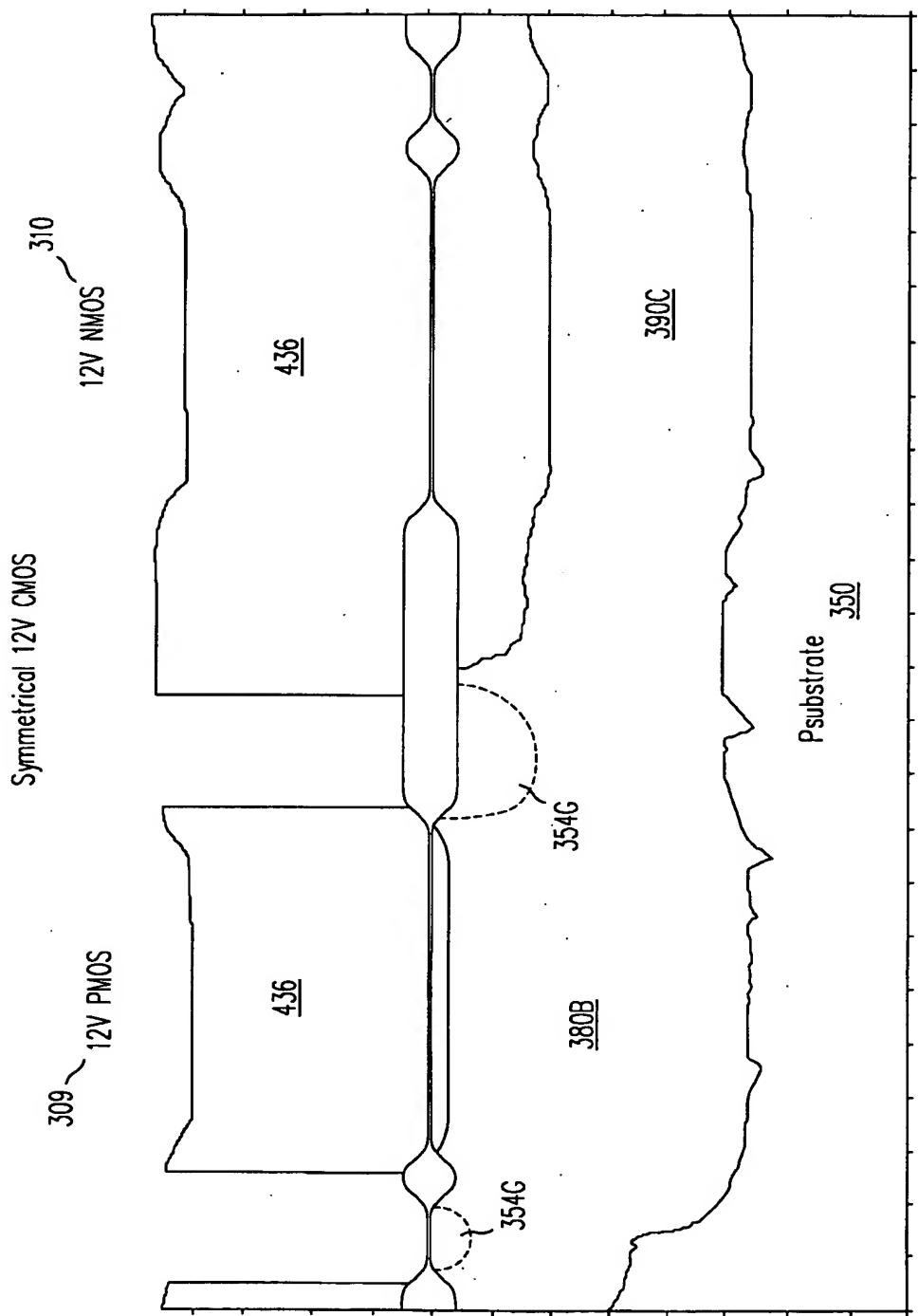


FIG. 40D



5V N Well Implant-First Stage

FIG. 40E

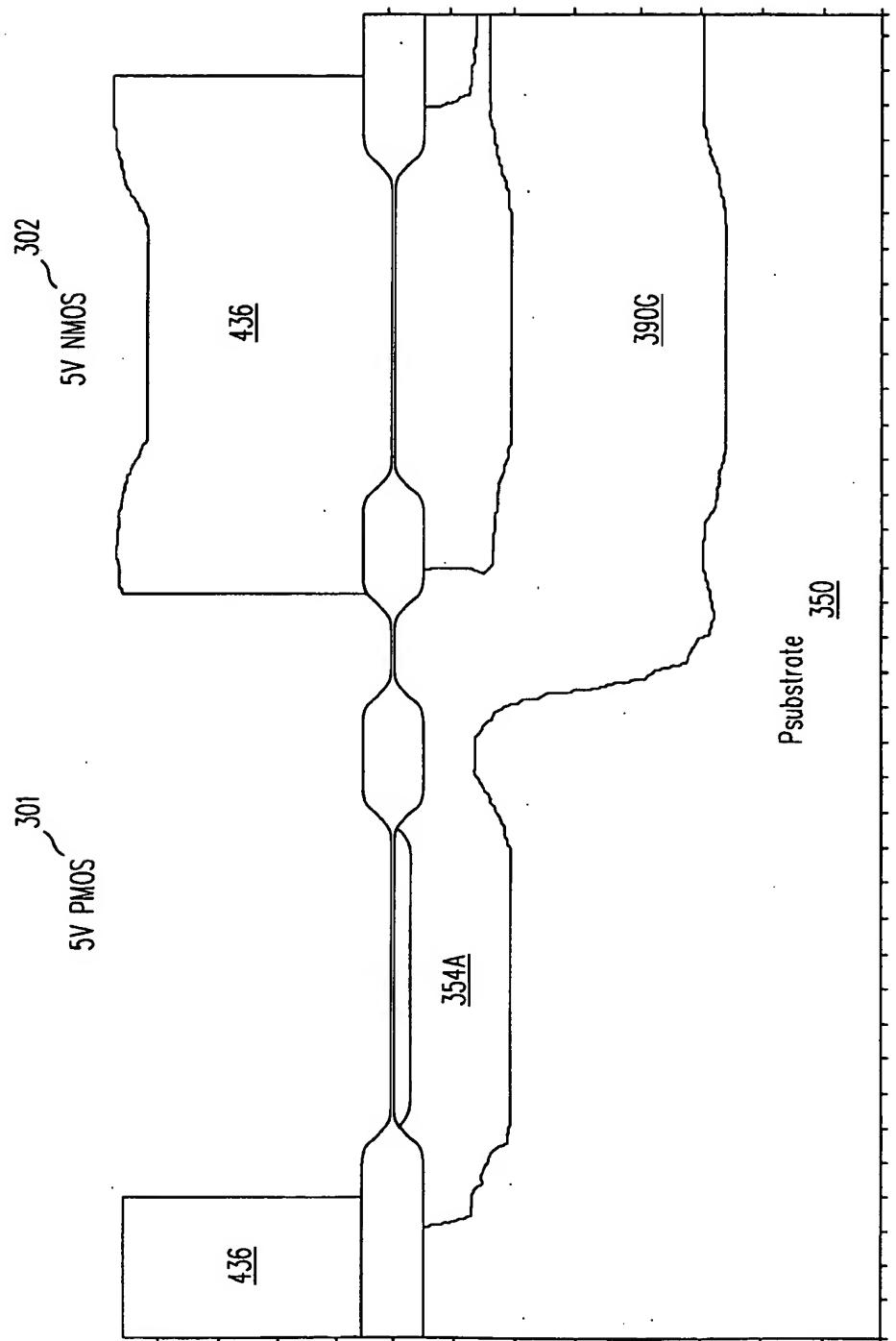


FIG. 41A

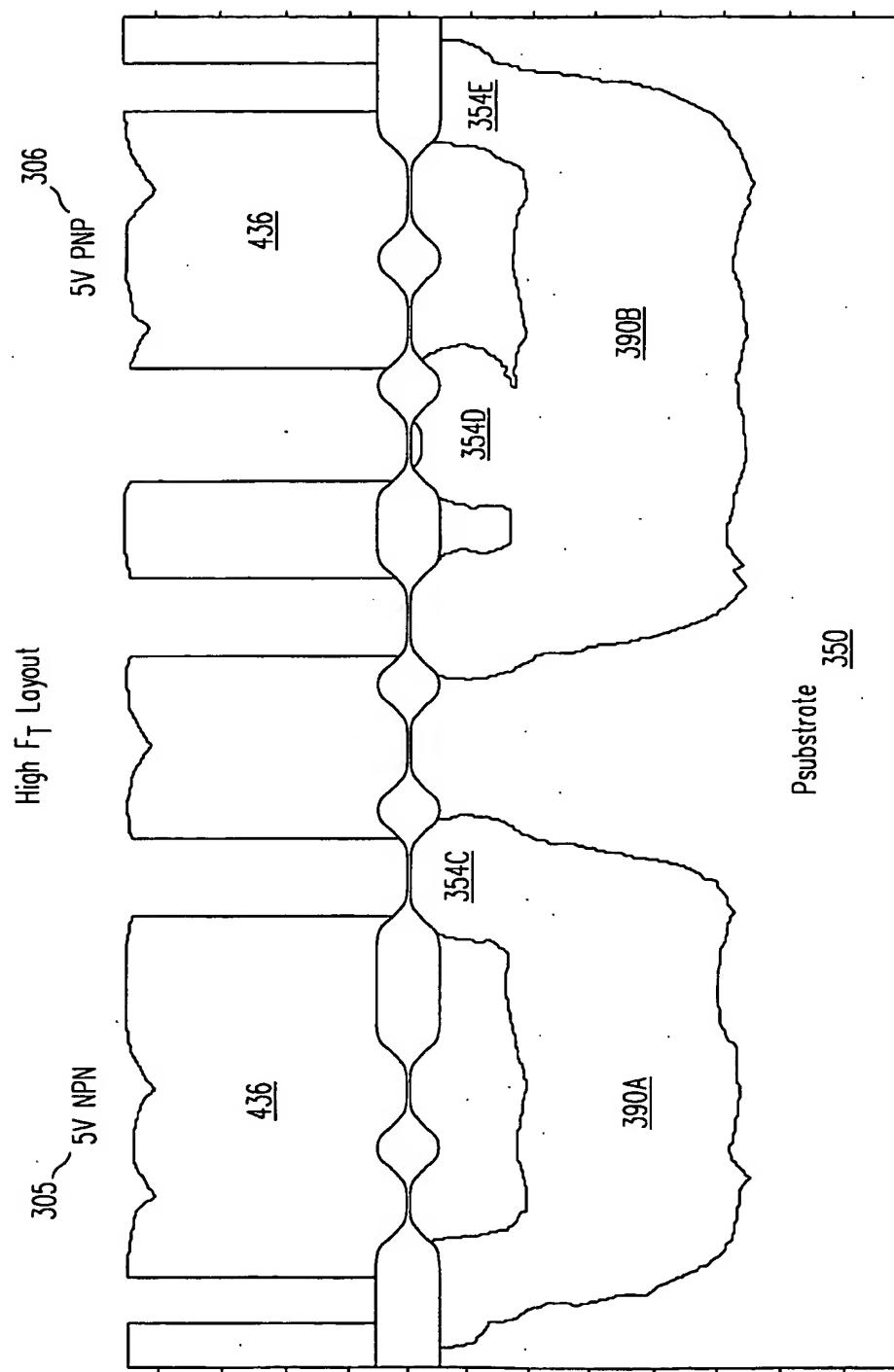
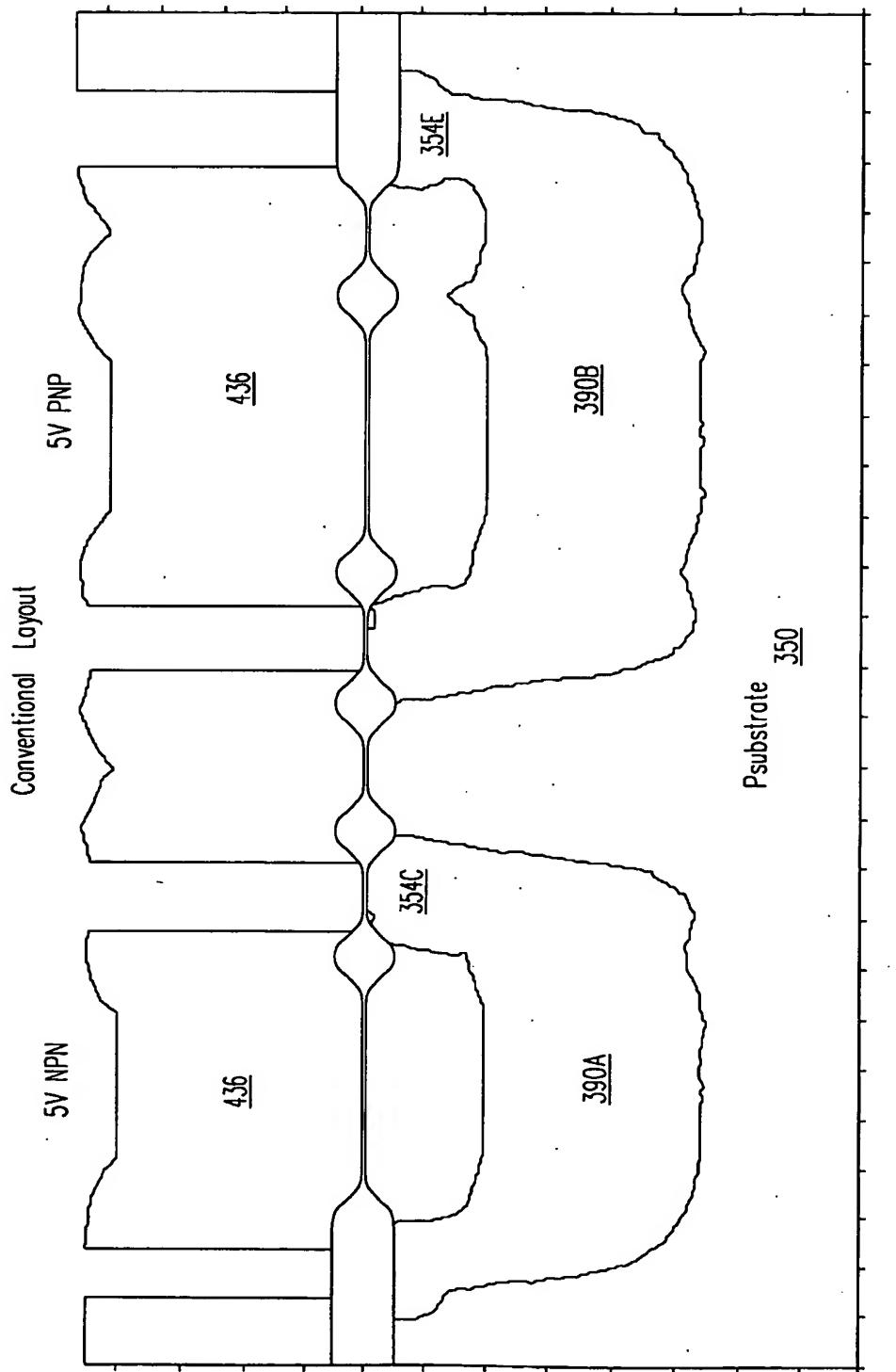
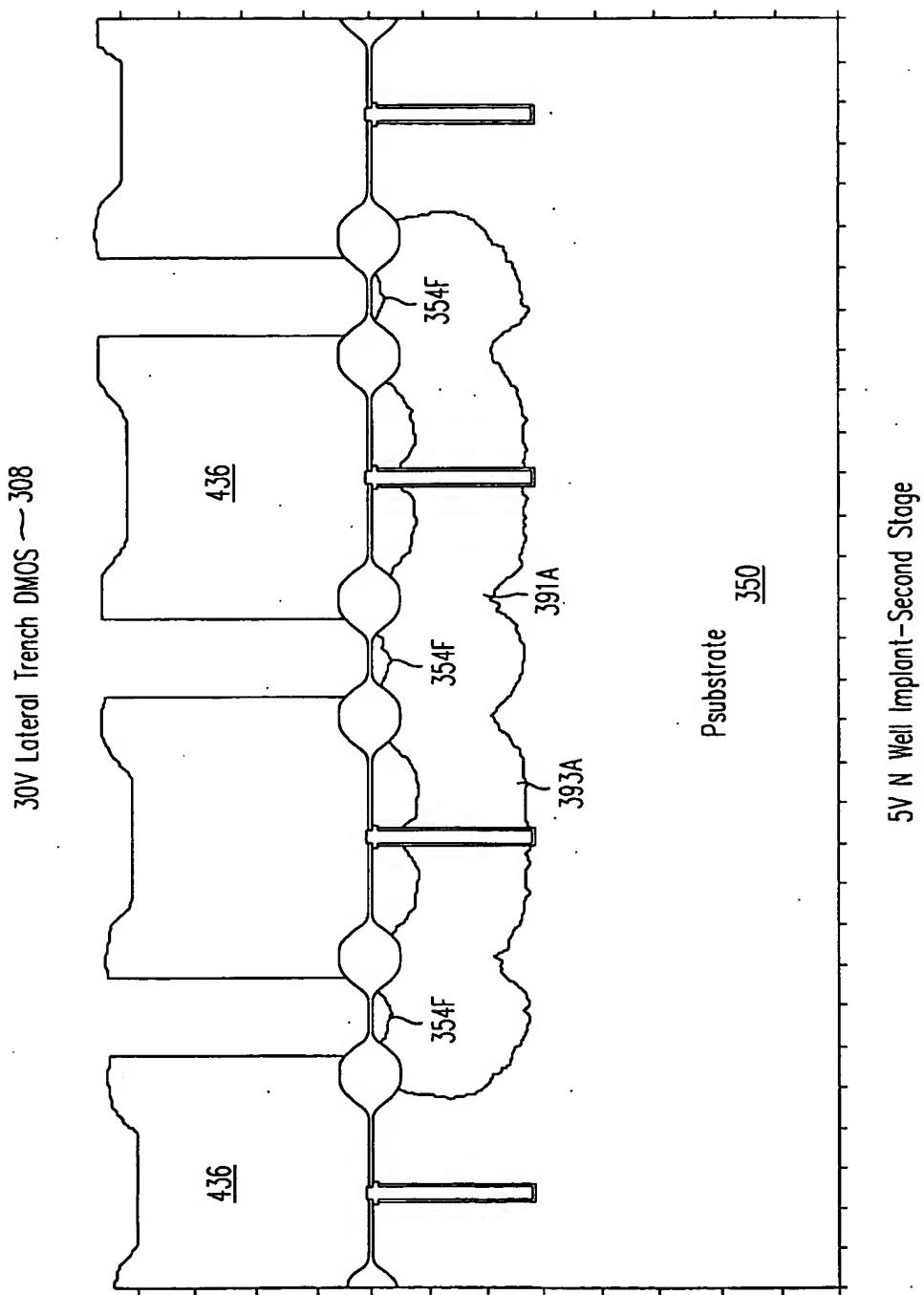


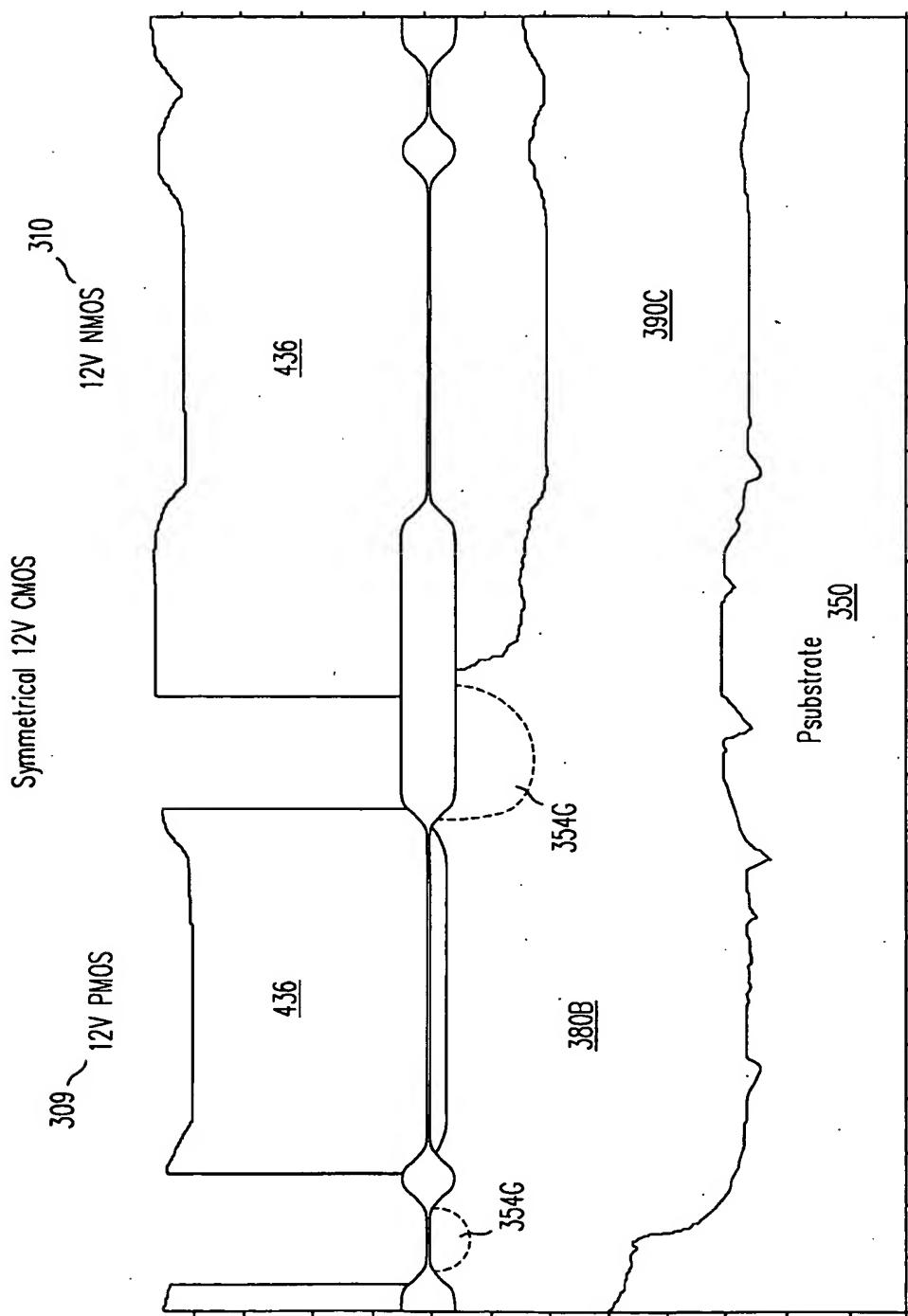
FIG. 41B



5V N Well Implant - Second Stage

FIG. 41C

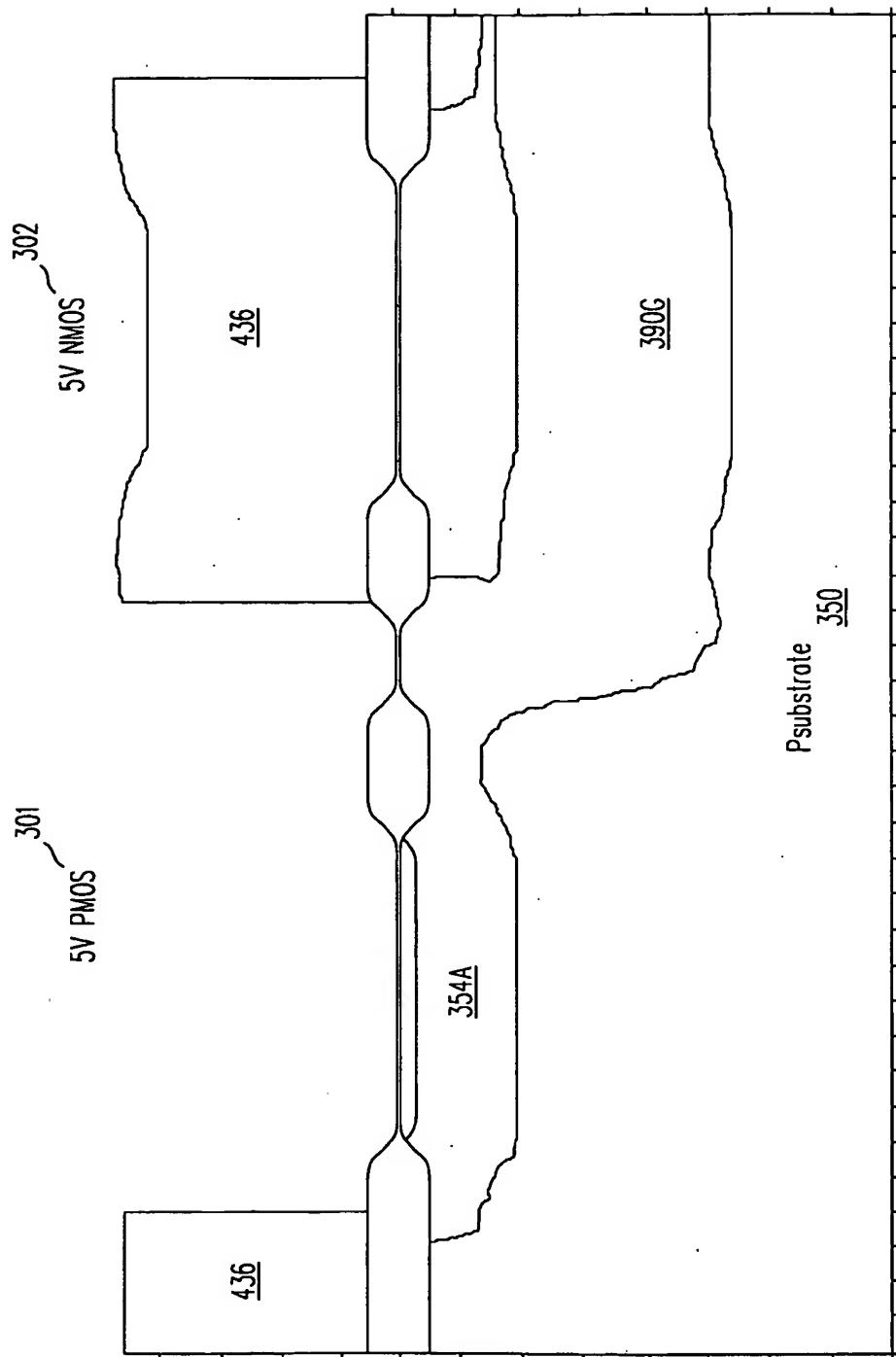




5V N Well Implant-Second Stage

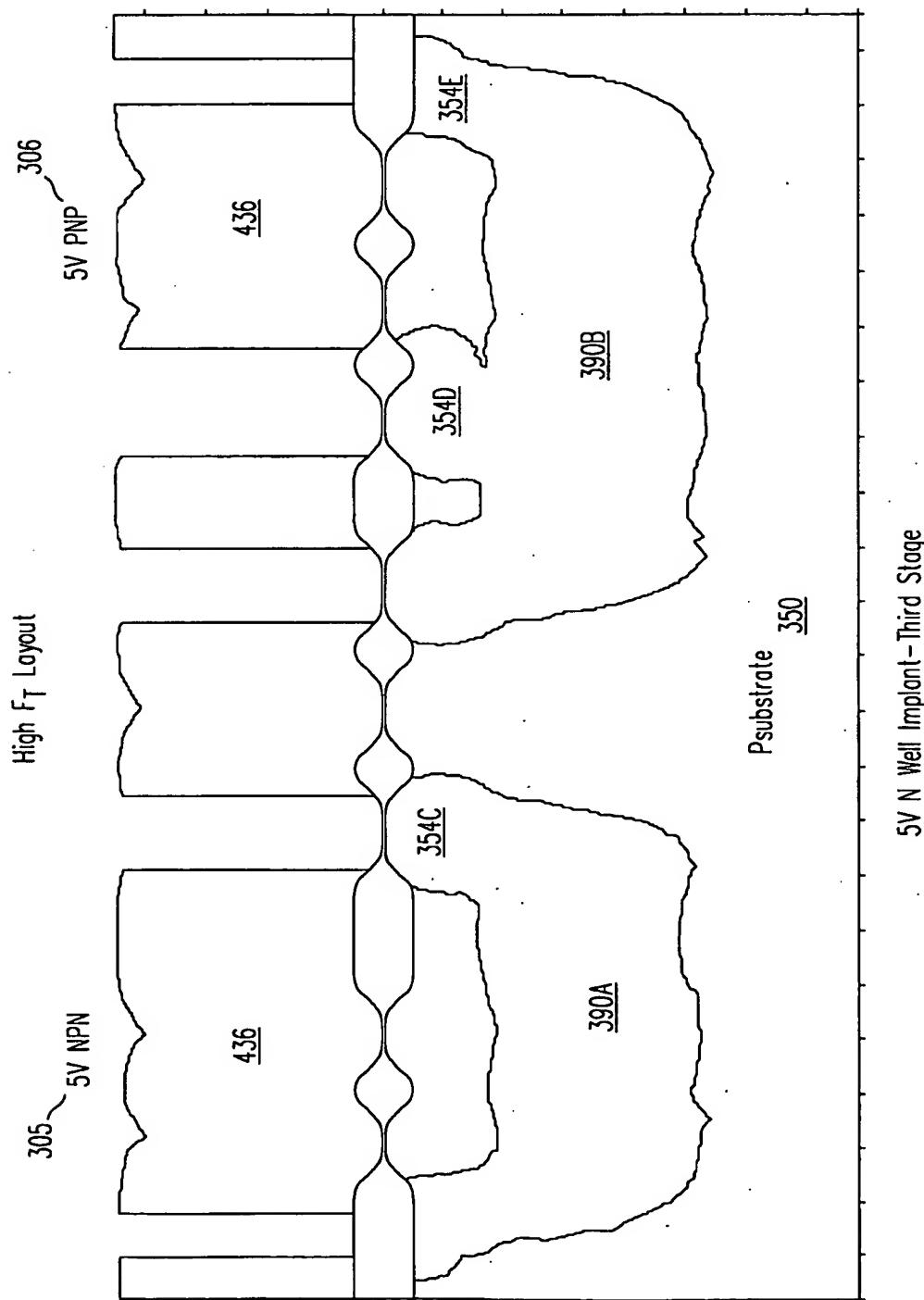
FIG. 41E

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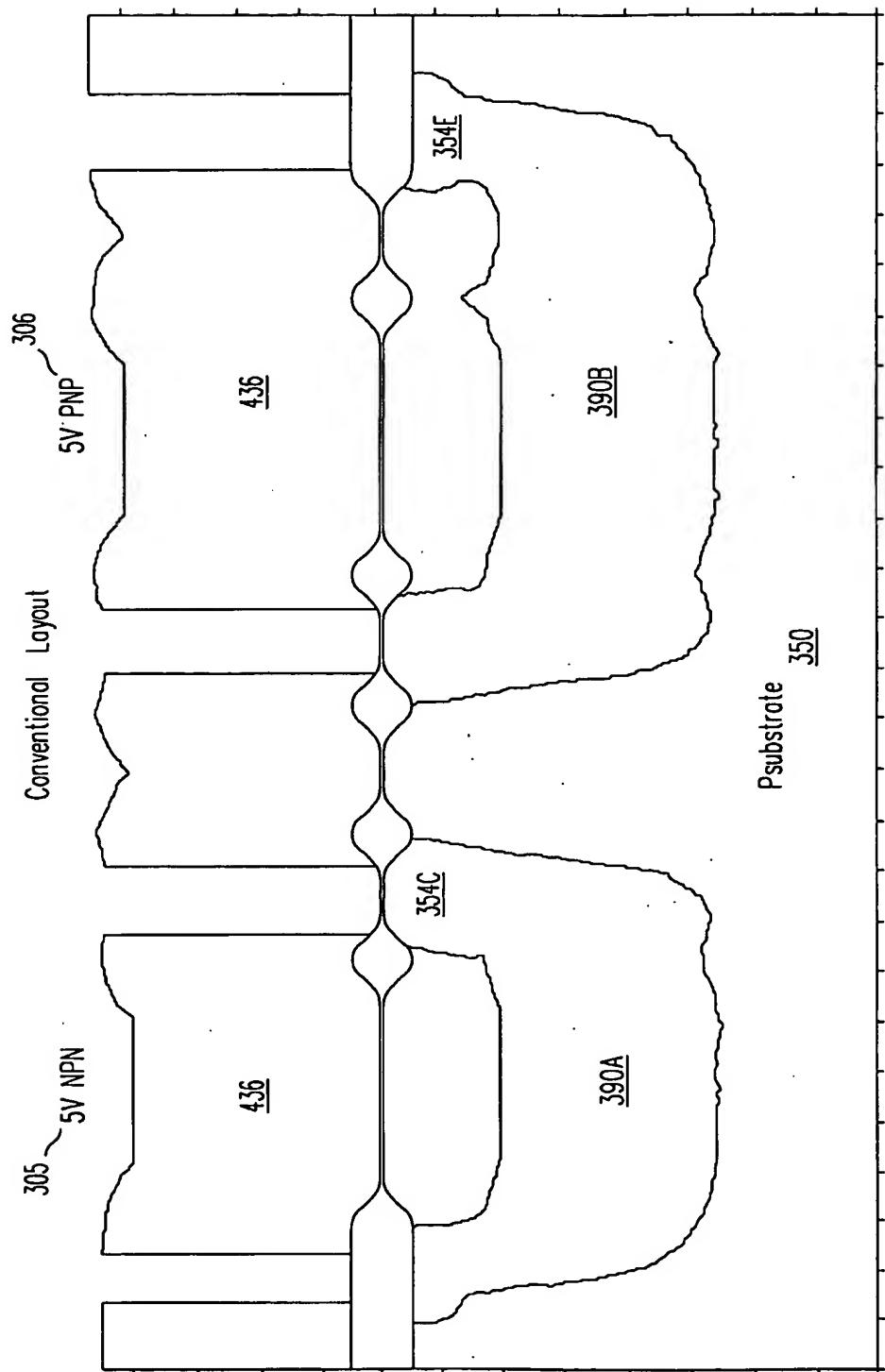
5V N Well Implant-Third Stage

FIG. 42A



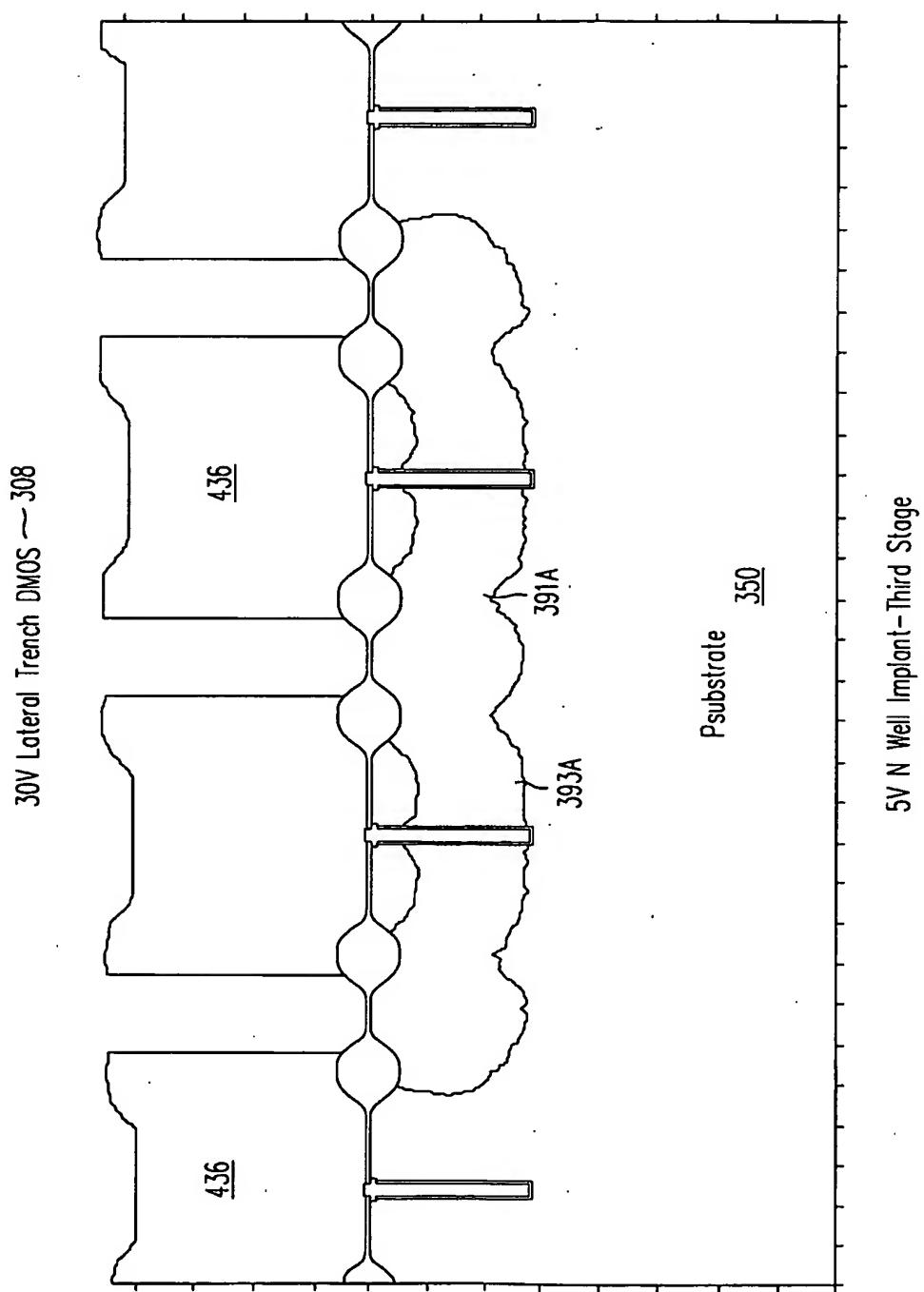
5V N Well Implant-Third Stage

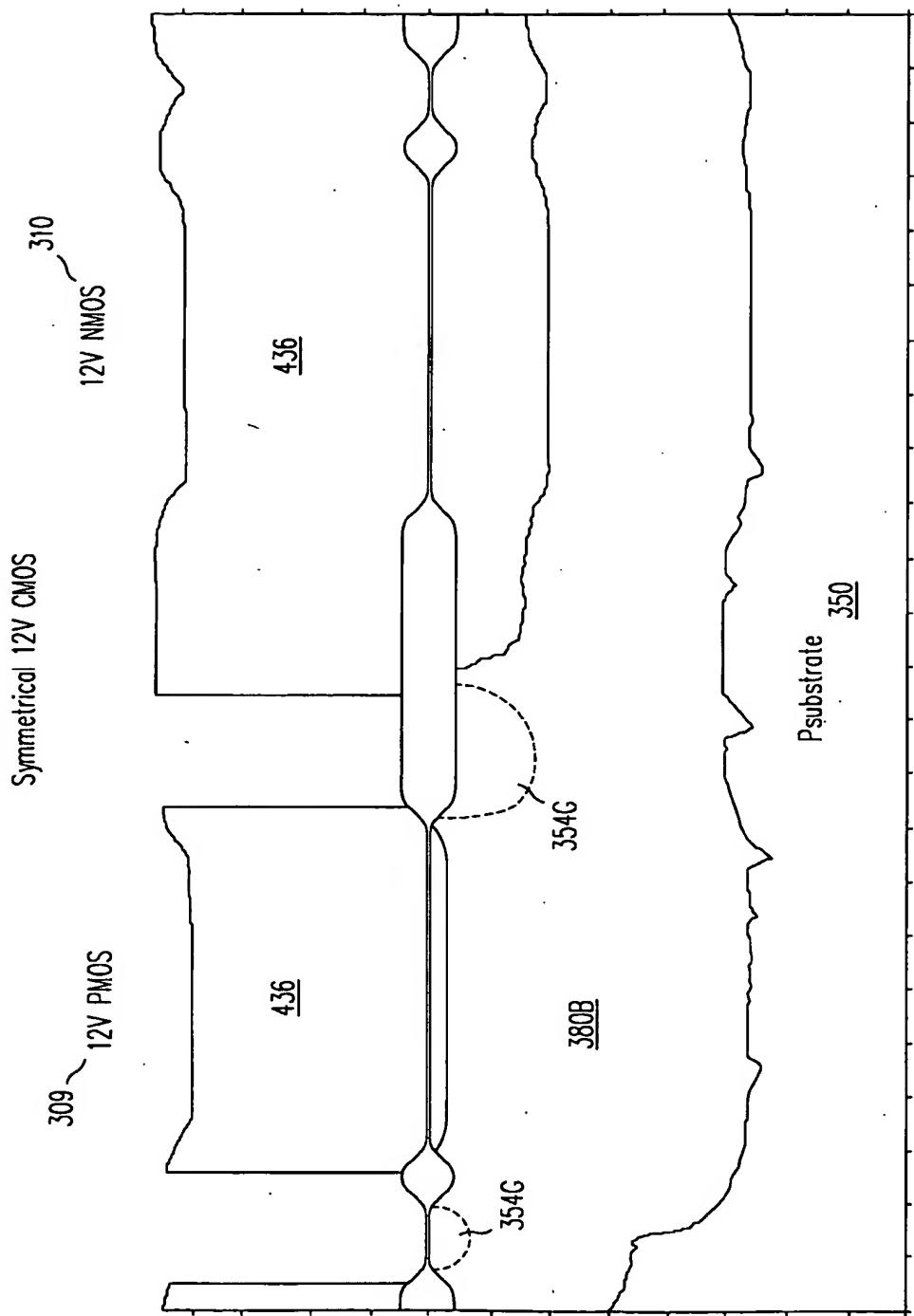
FIG. 42B



5V N Well Implant- Third Stage

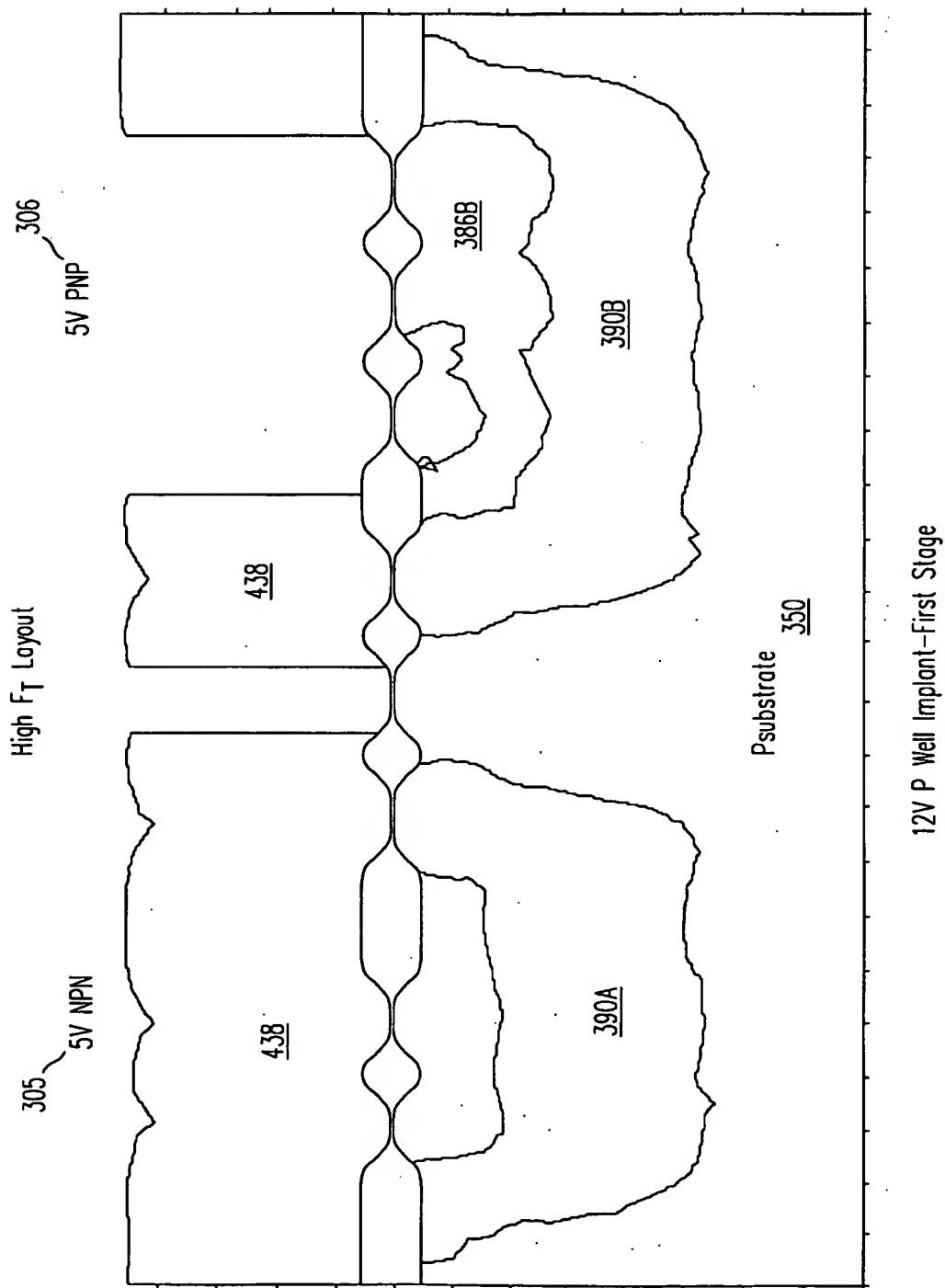
FIG. 42C





5V N Well implant-Third Stage

FIG. 42E



12V P Well Implant-First Stage

FIG. 43B

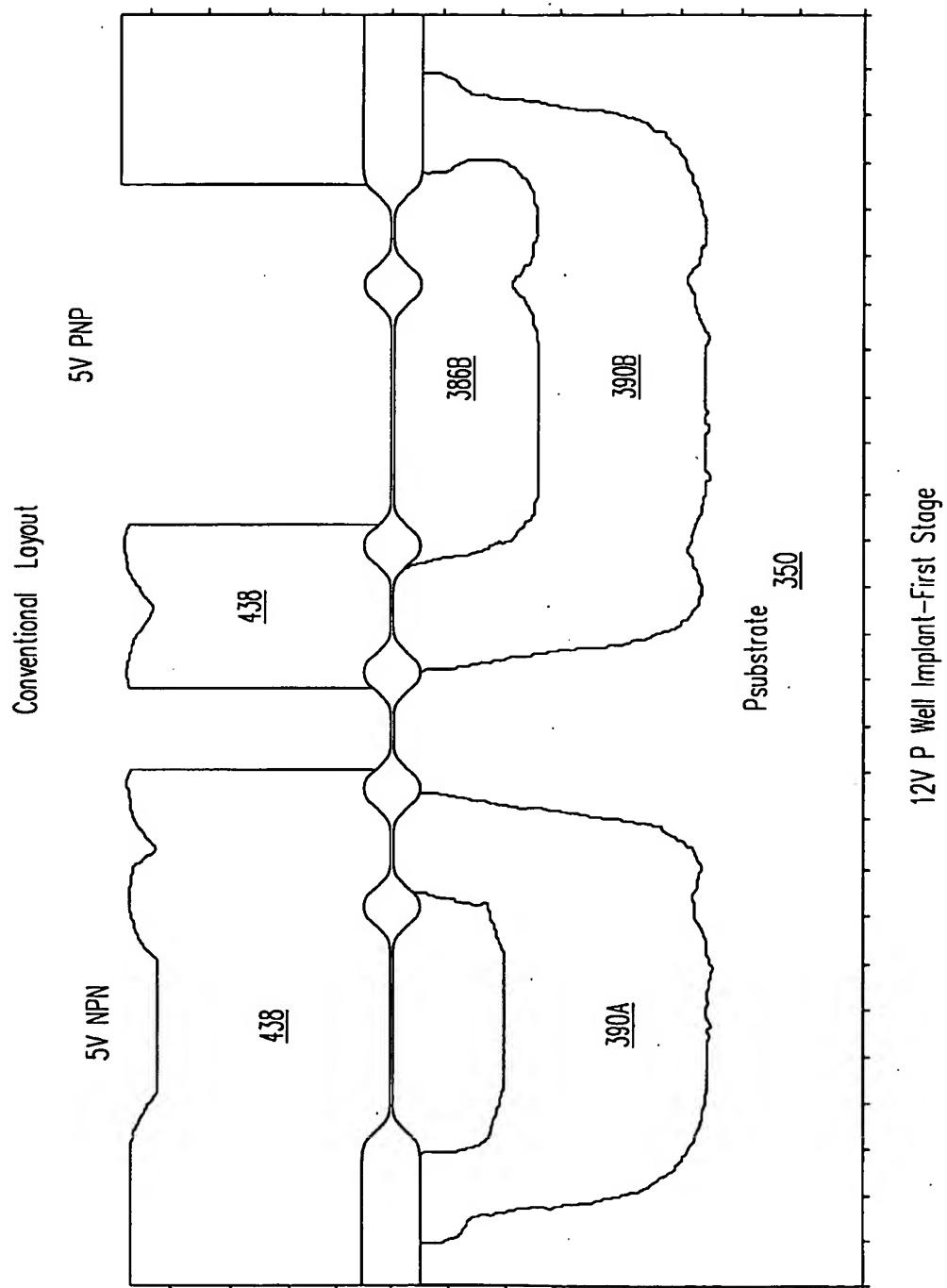


FIG. 43C

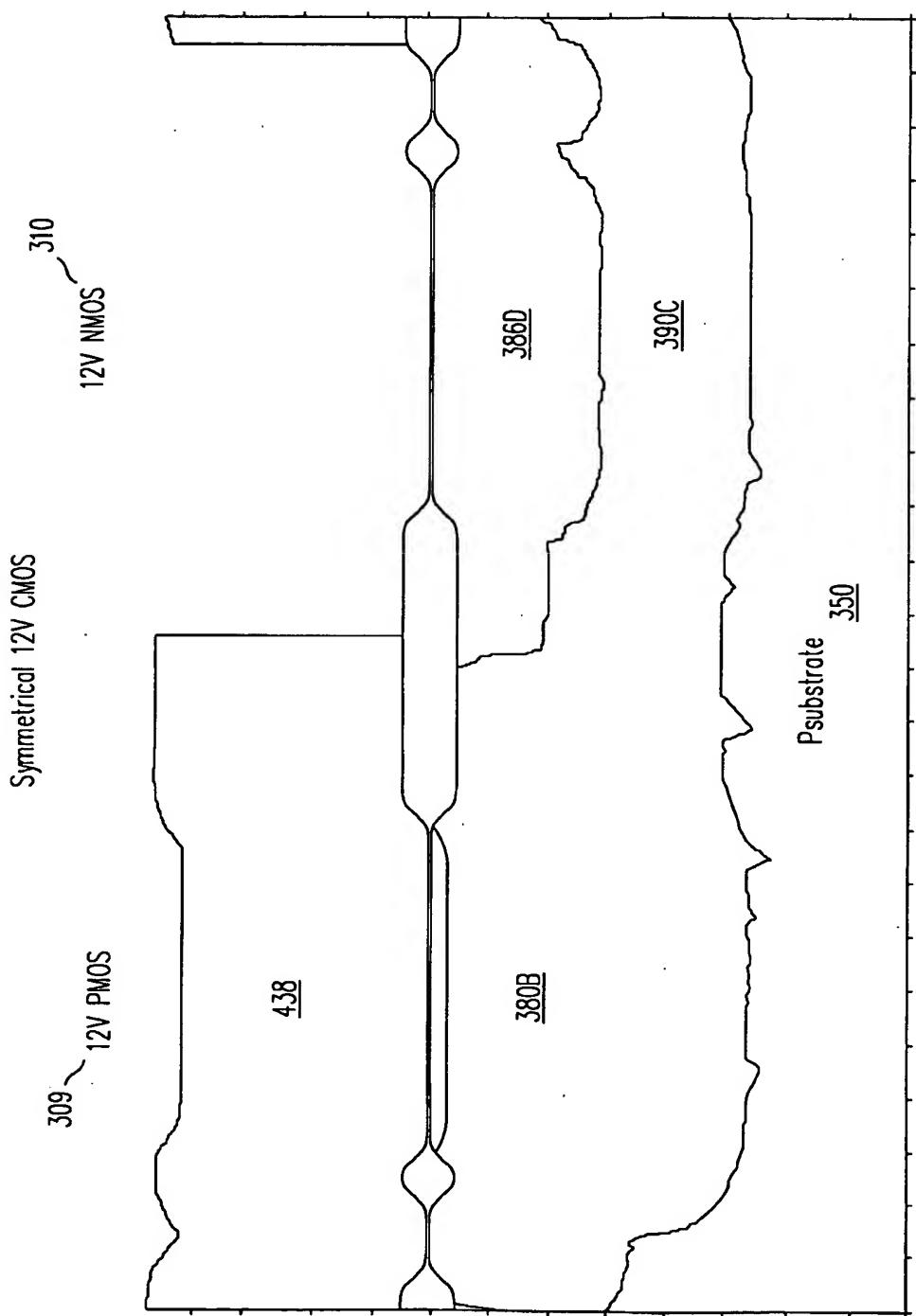
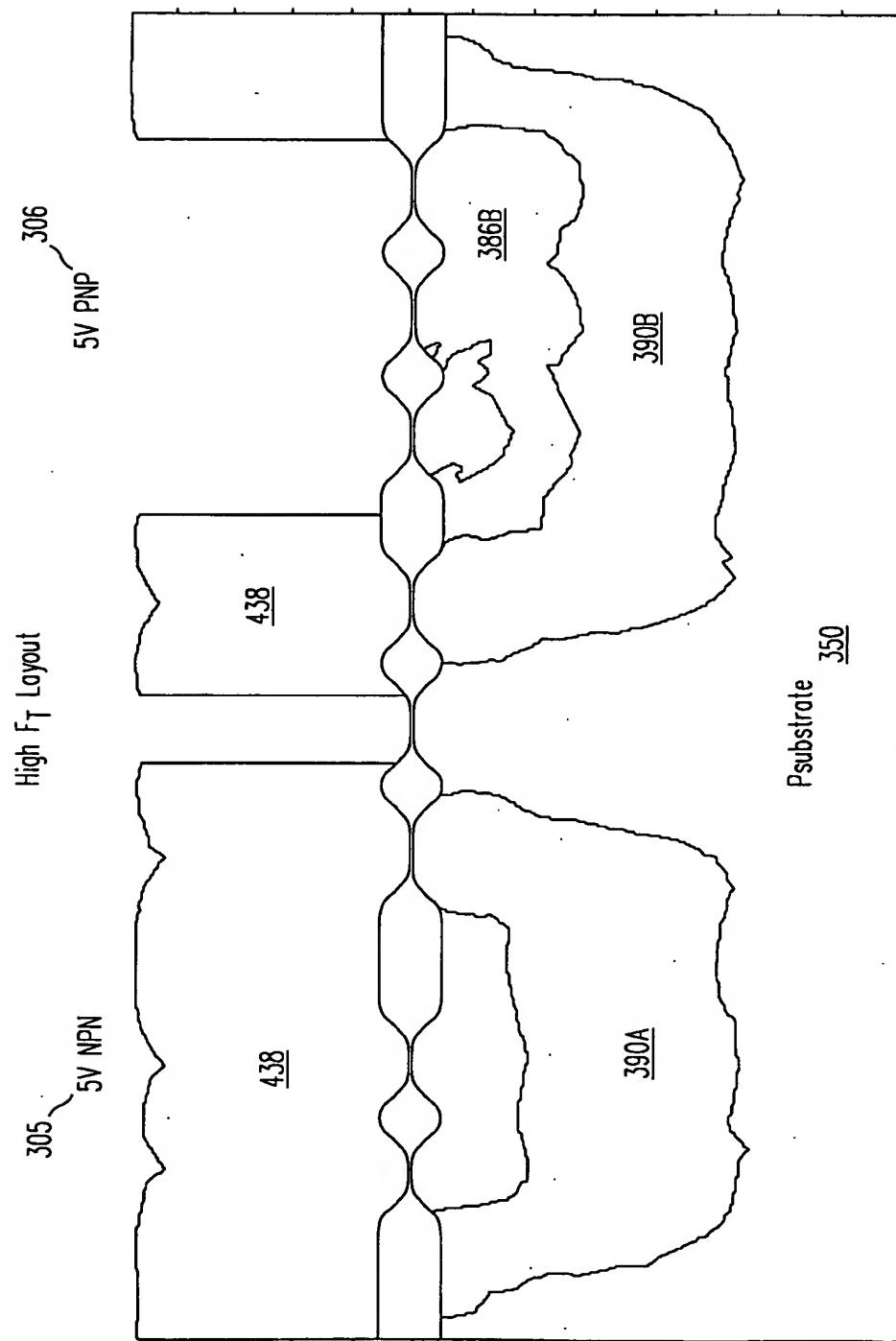
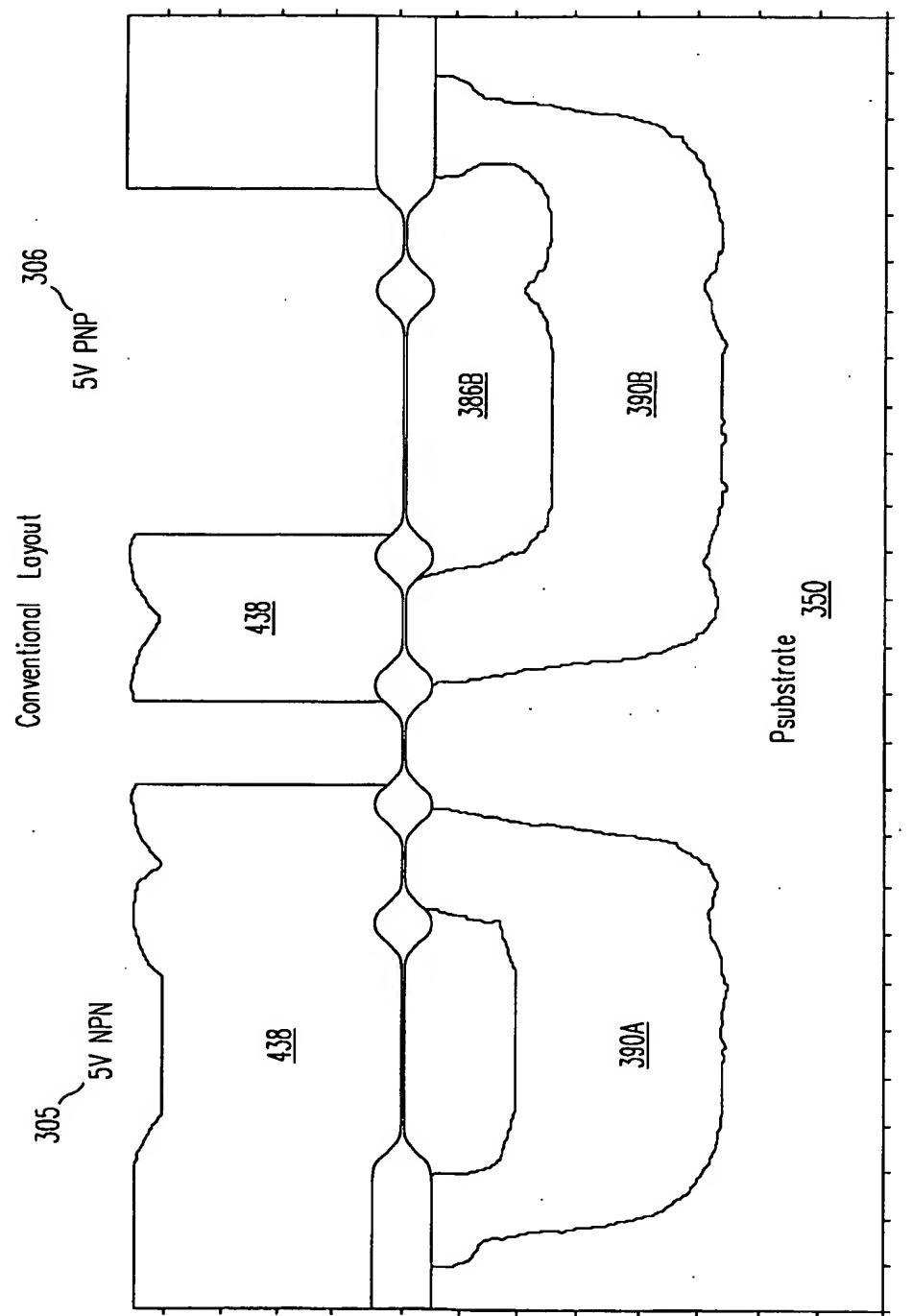


FIG. 43E



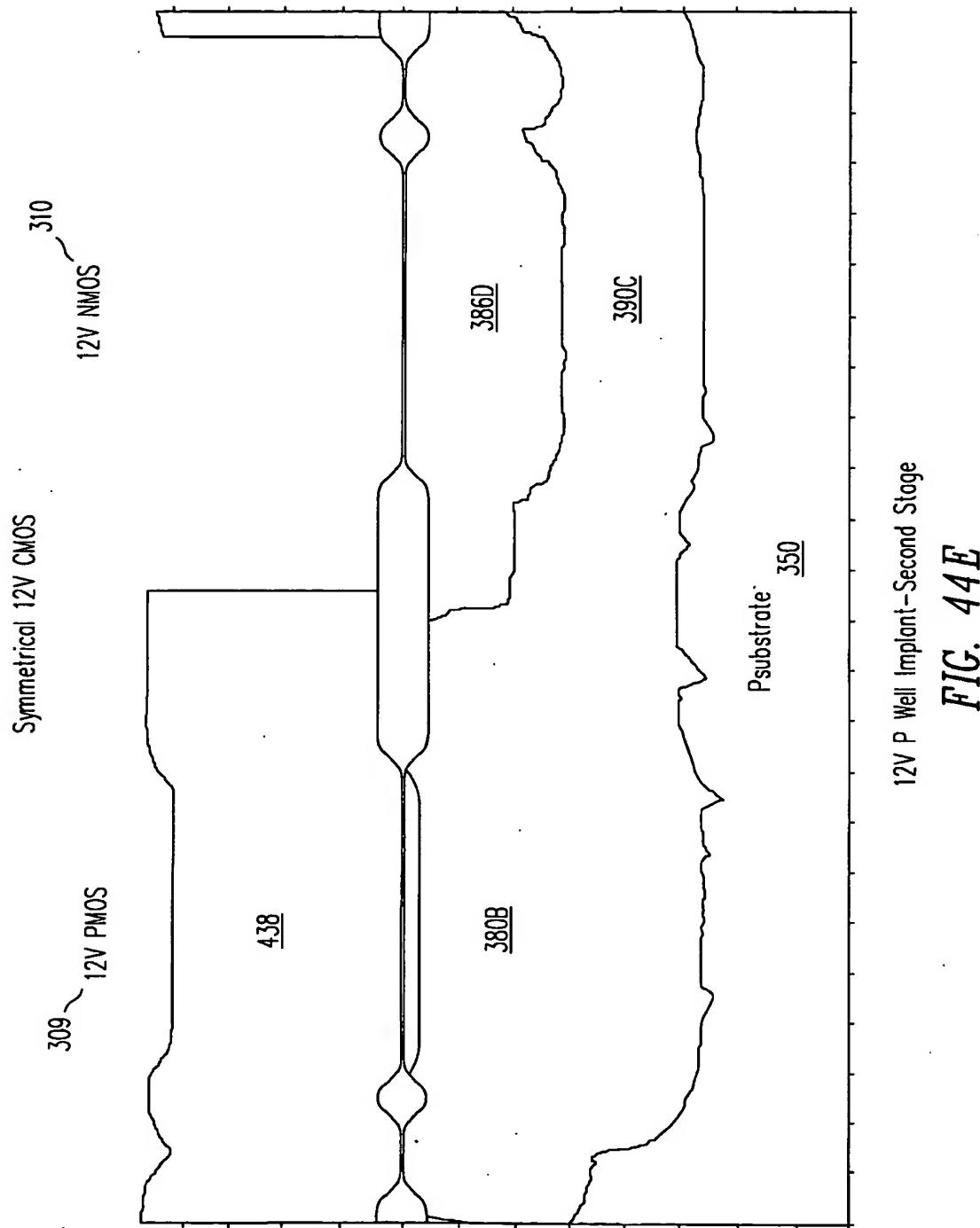
12V P Well Implant-Second Stage

FIG. 44B

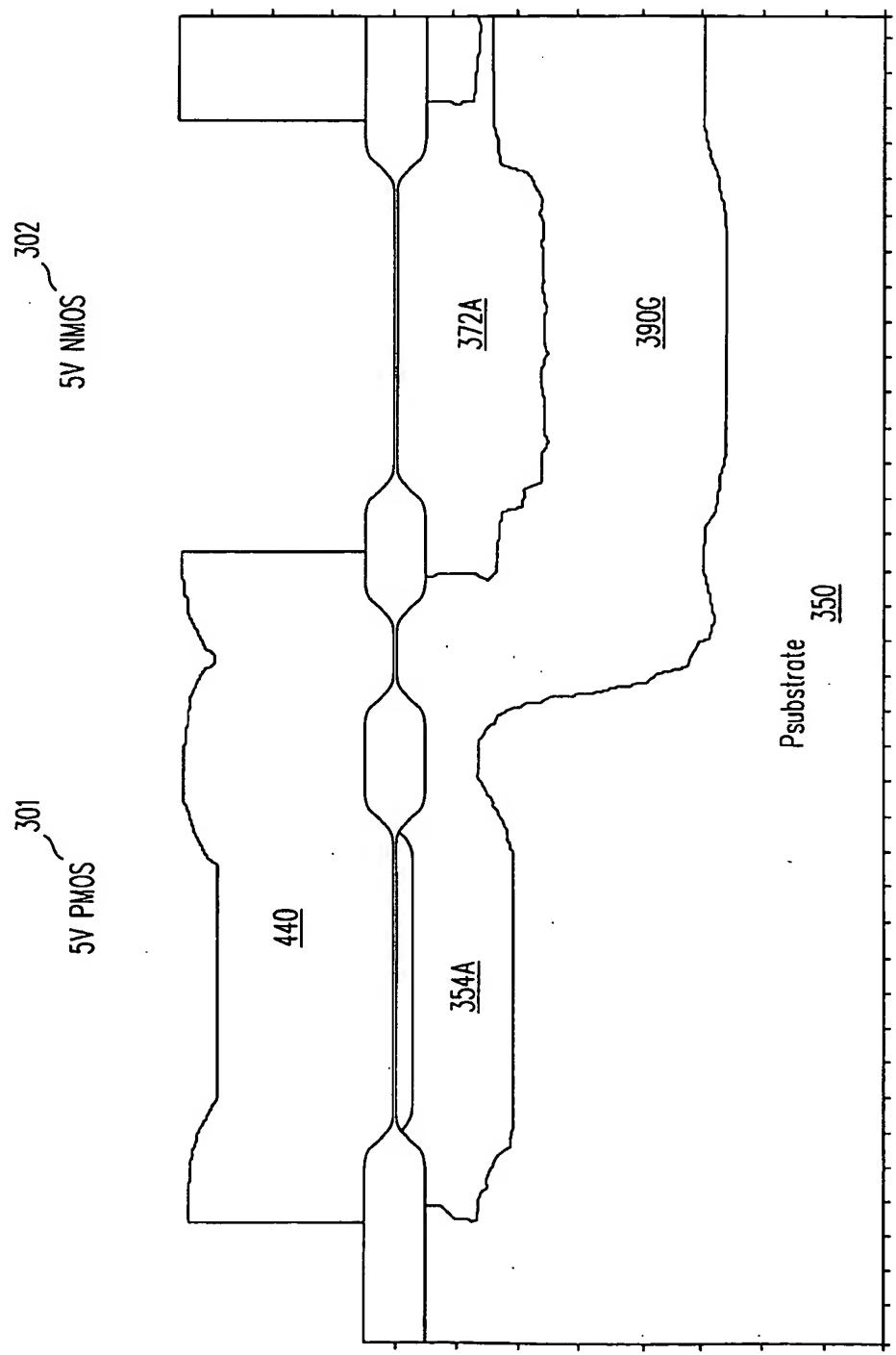


12V P Well Implant-Second Stage

FIG. 44C

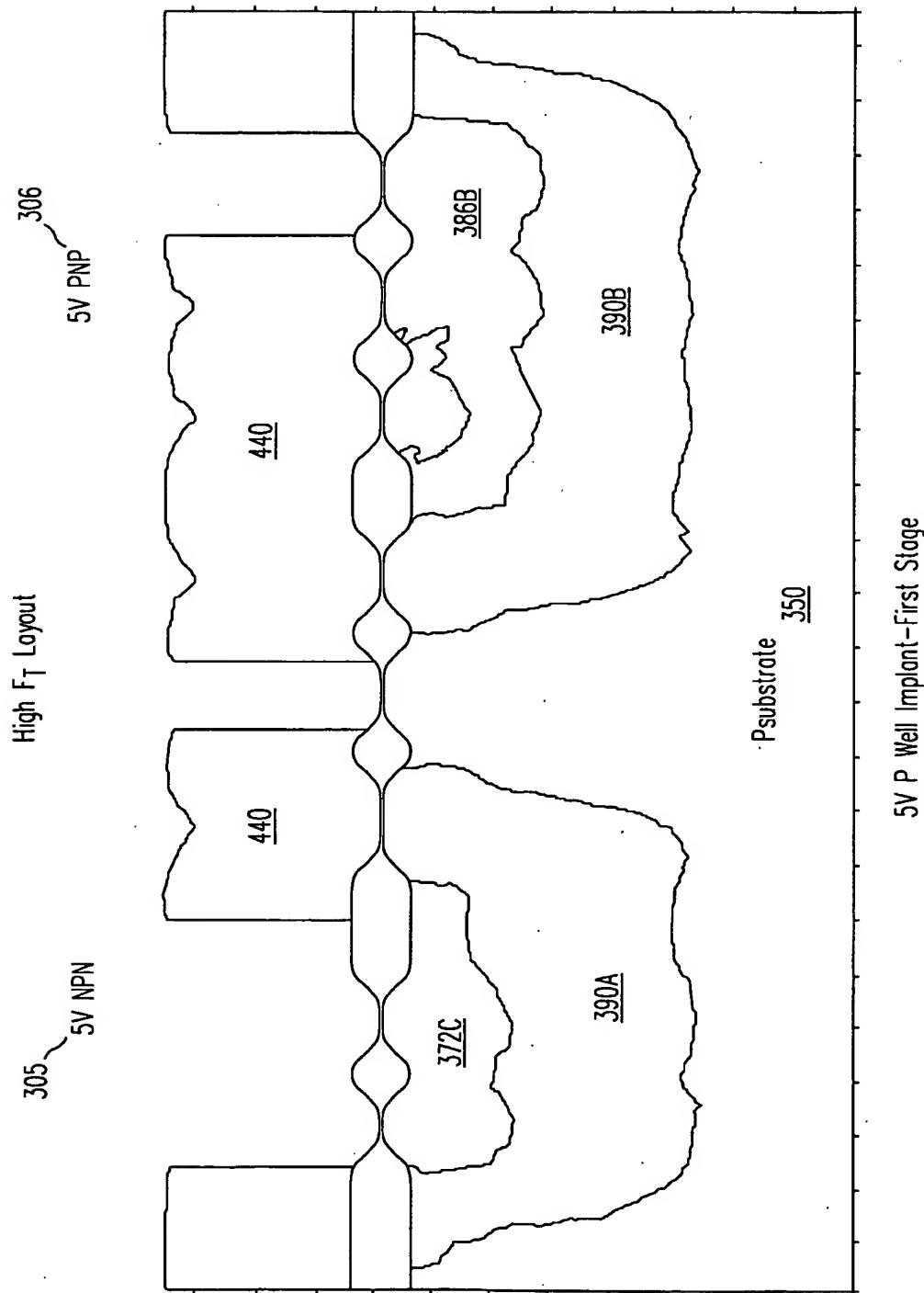


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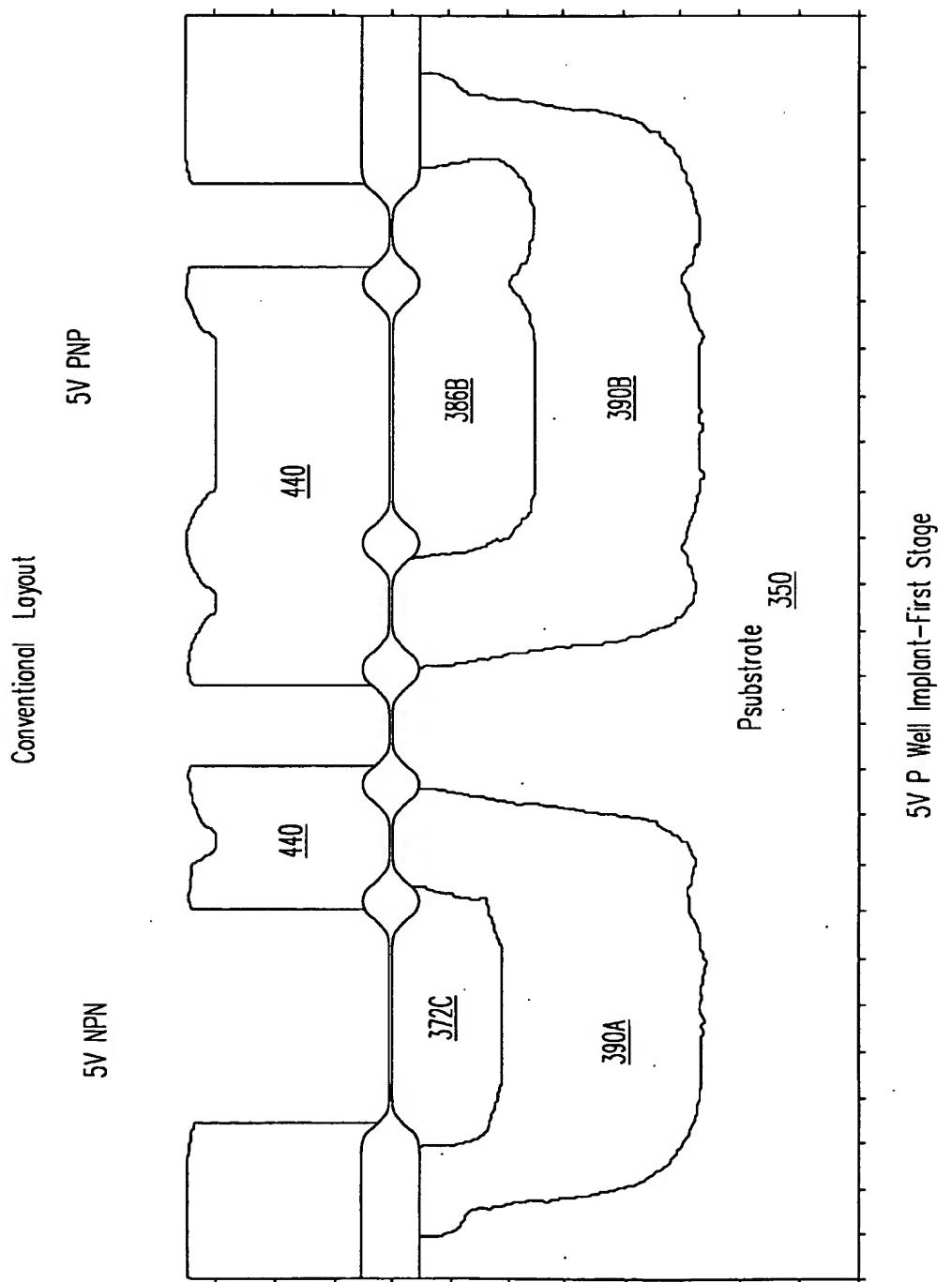
5V P Well Implant-First Stage

FIG. 45A



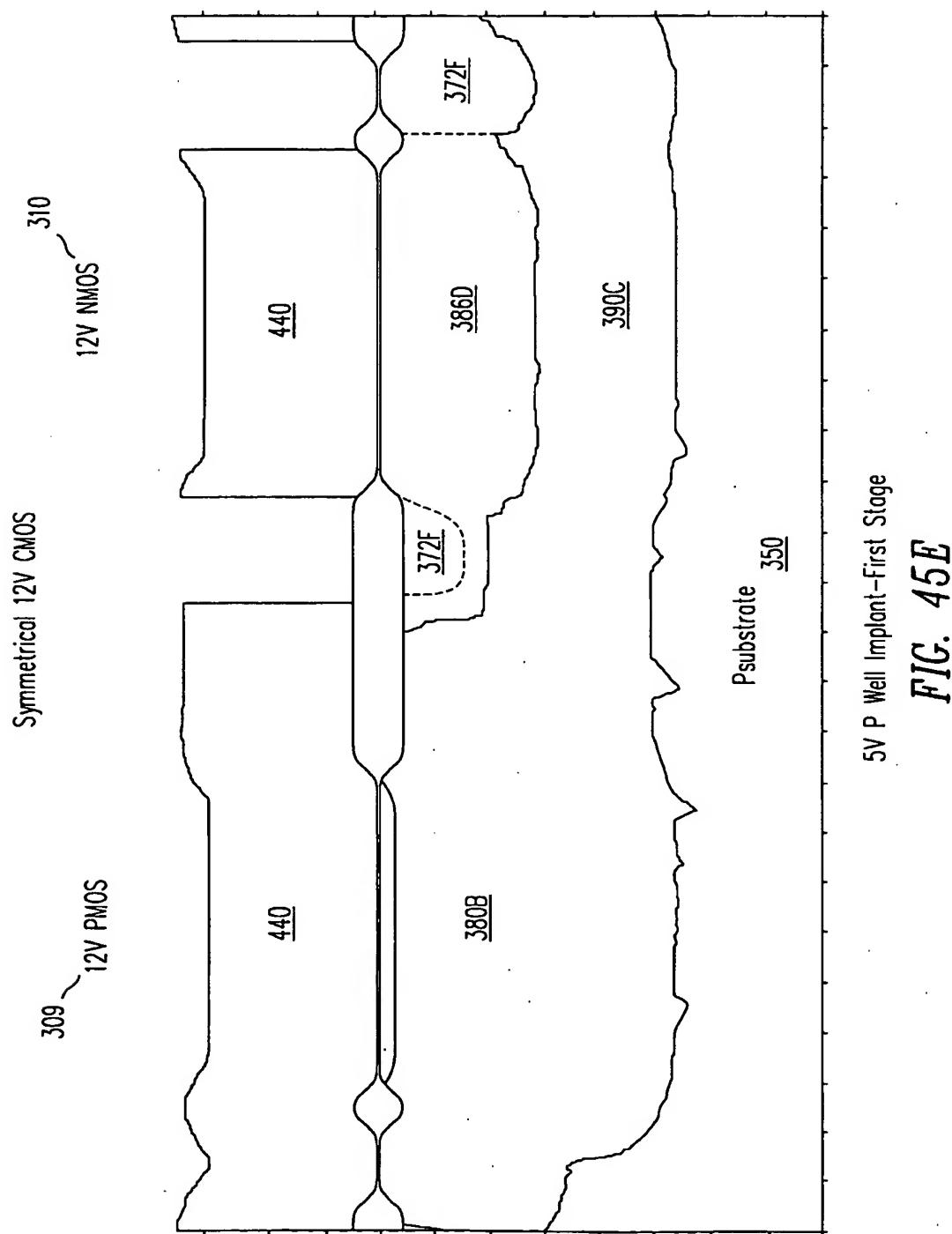
5V P Well Implant-First Stage

FIG. 45B

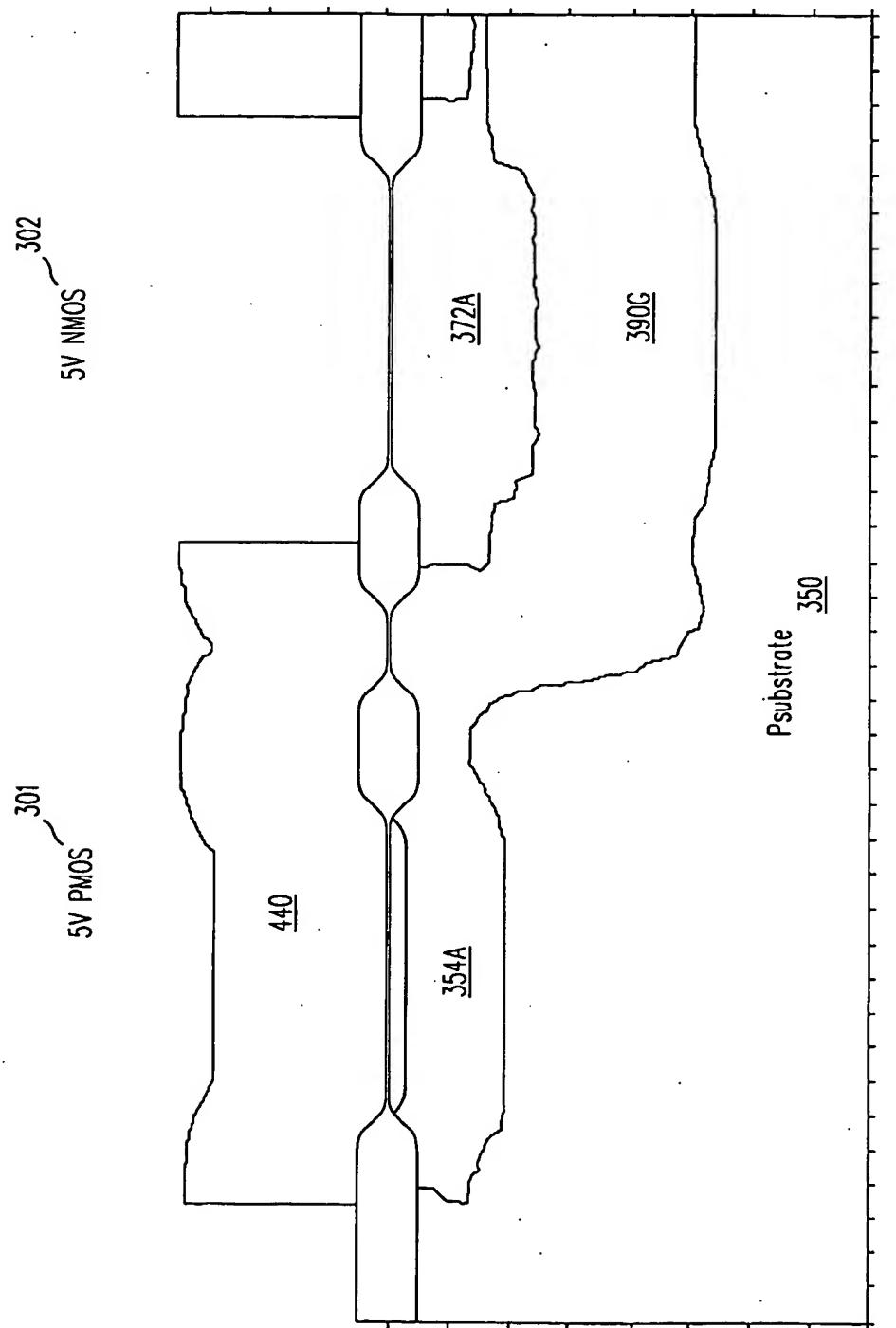


5V P Well Implant-First Stage

FIG. 45C

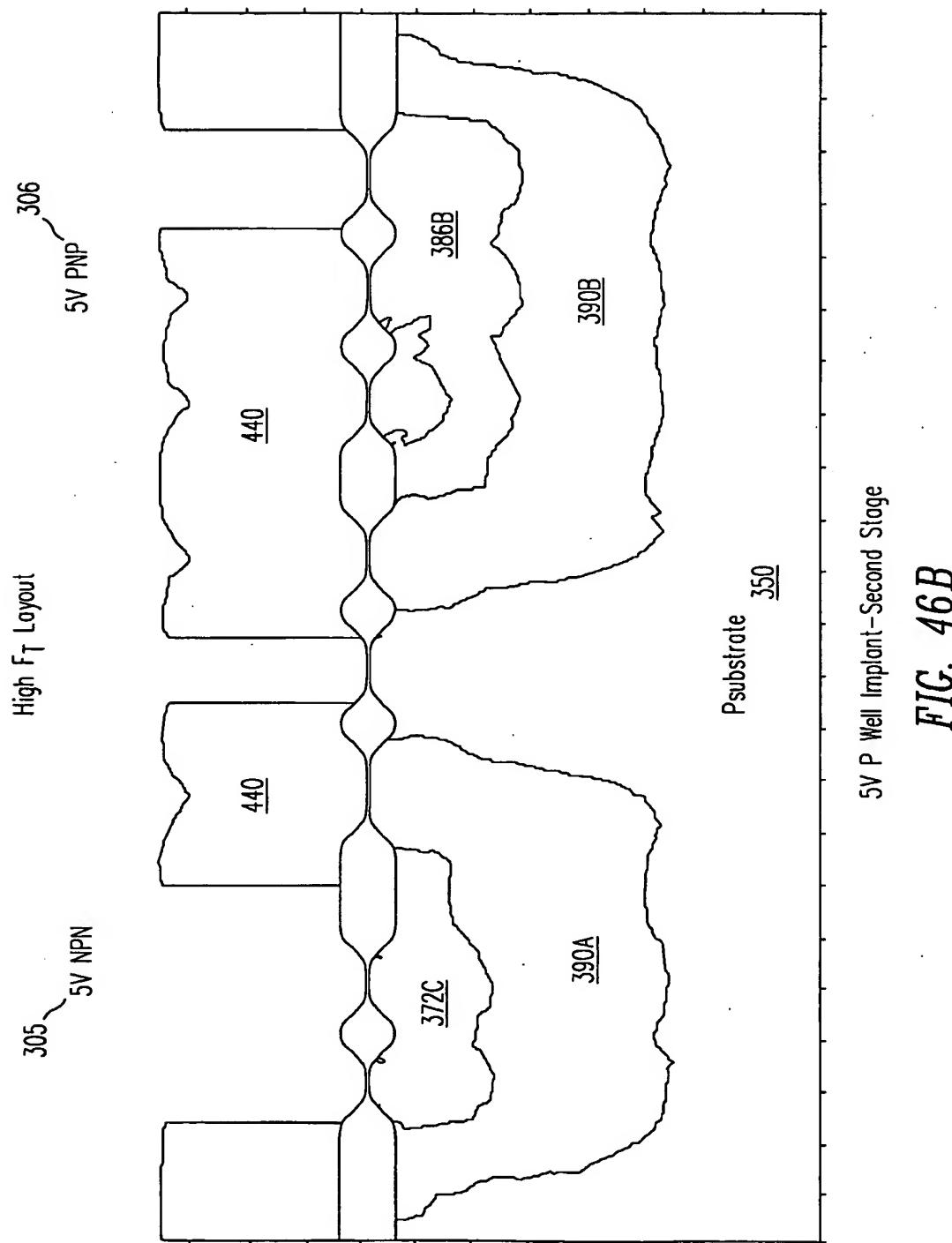


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5V P Well Implant - Second Stage

FIG. 46A



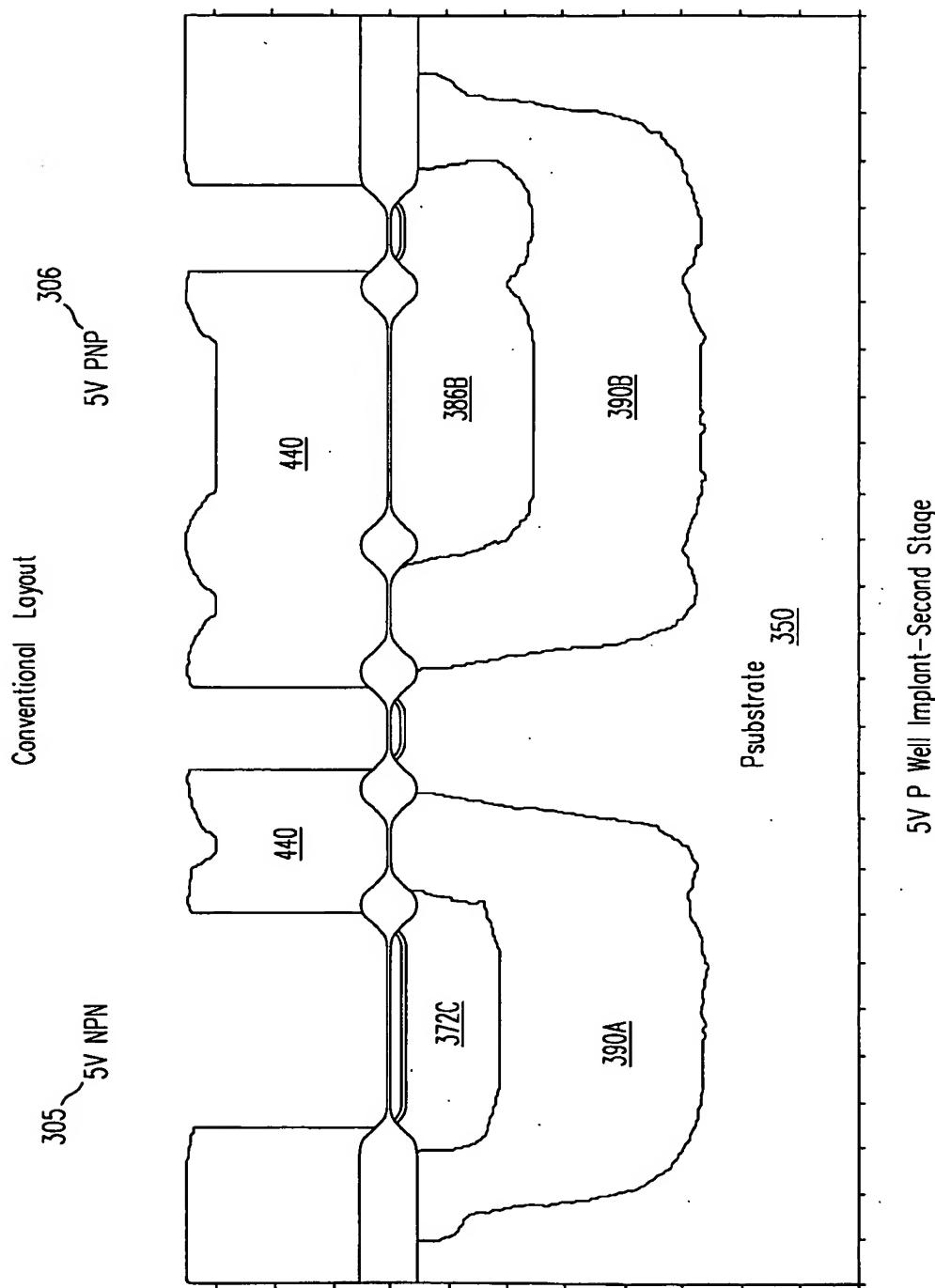
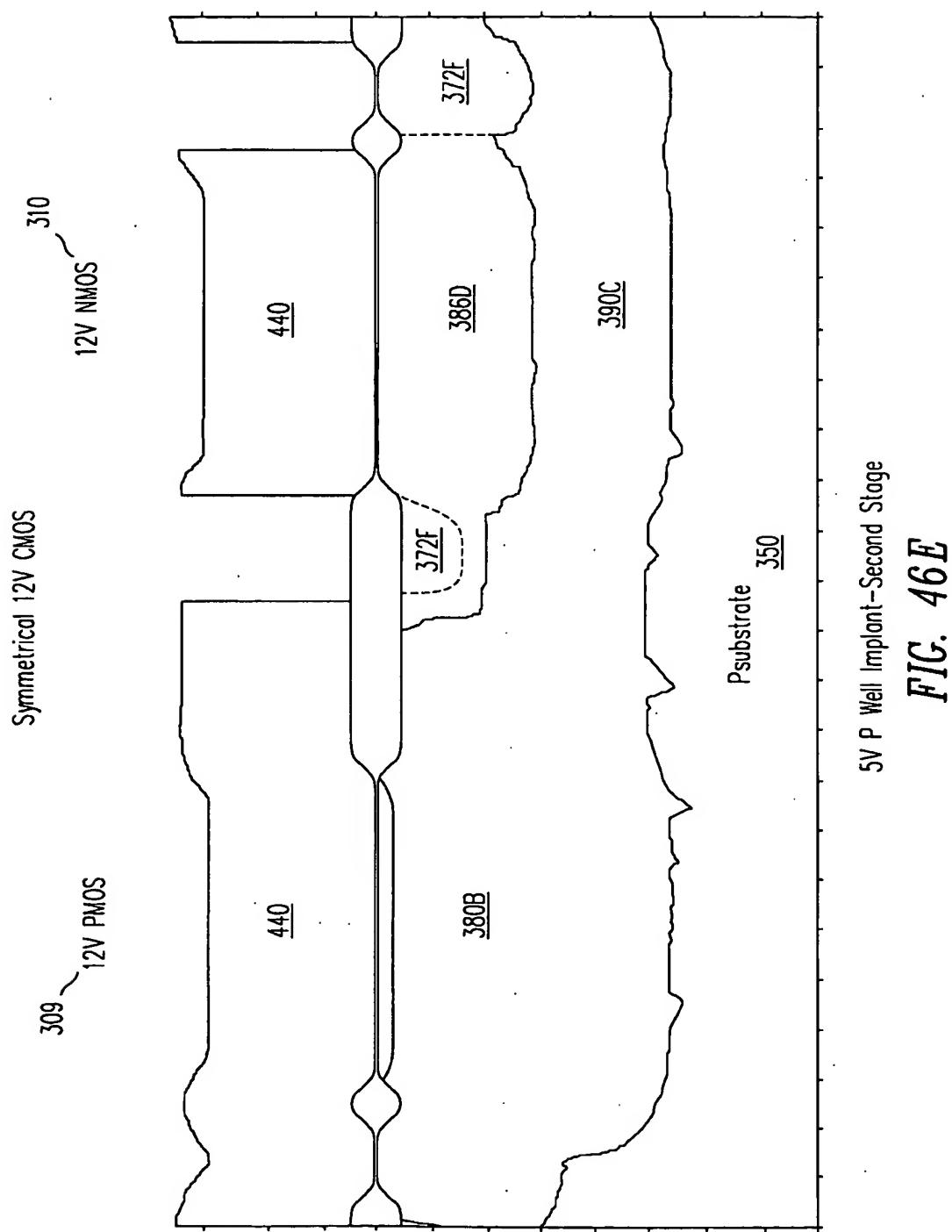


FIG. 46C



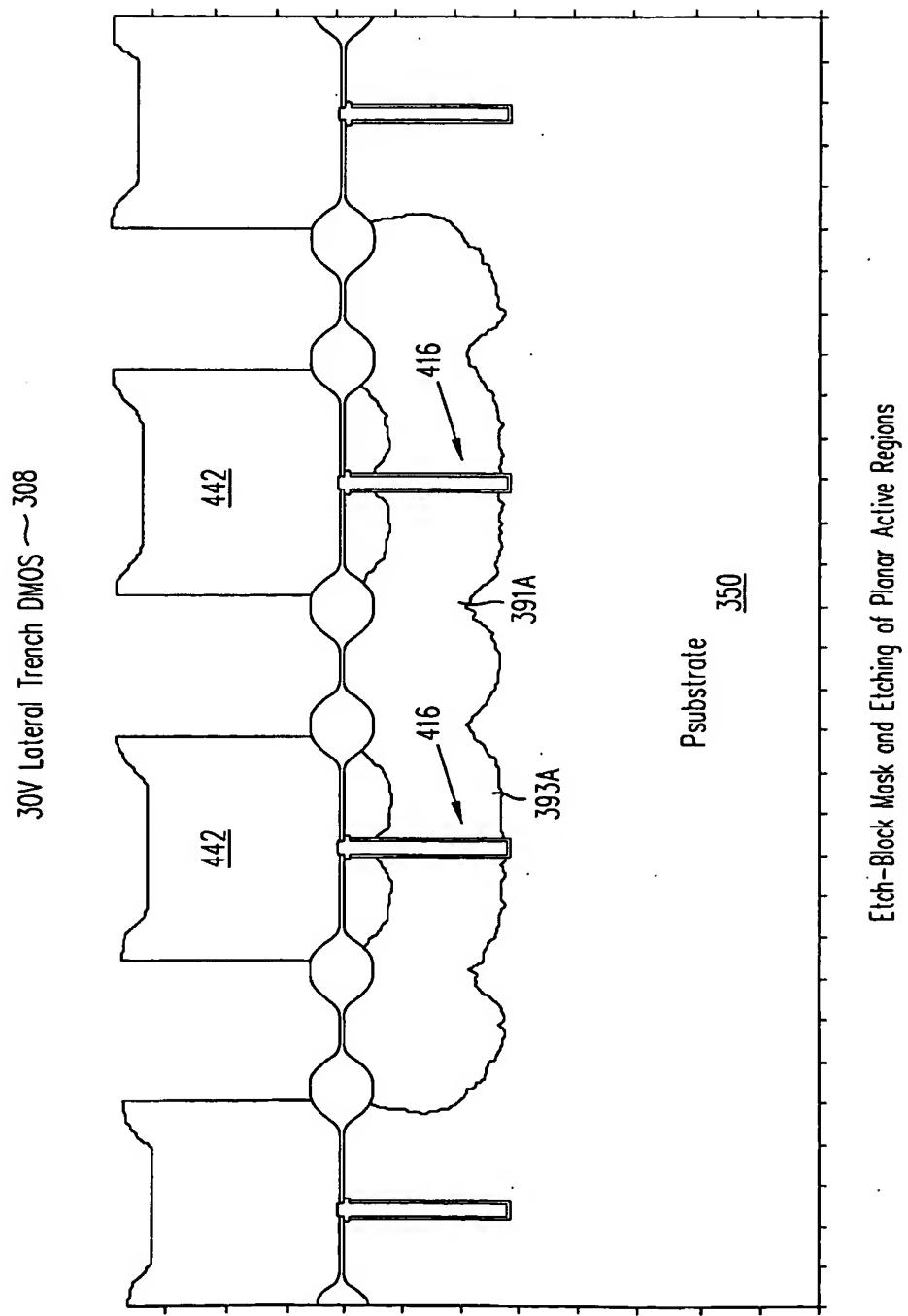
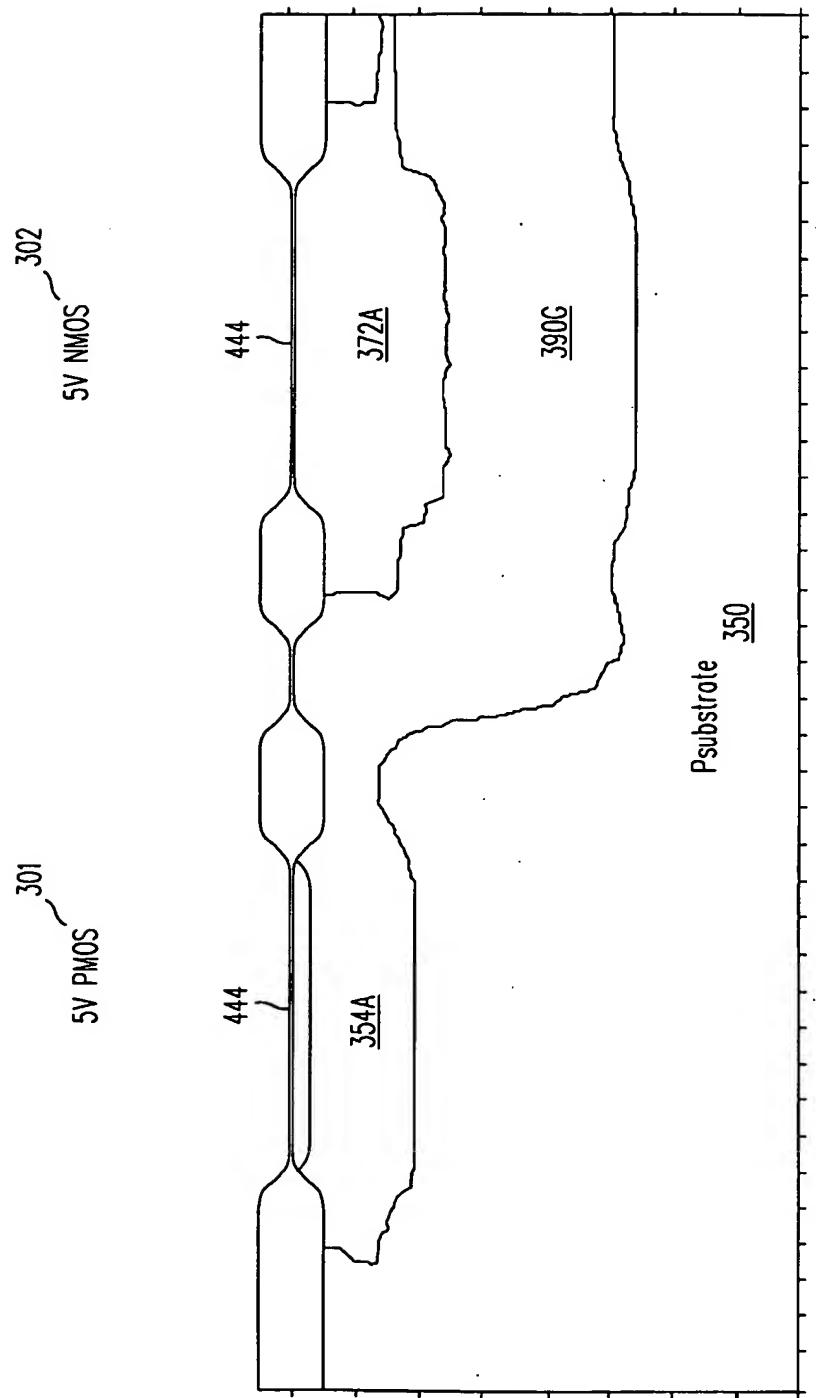
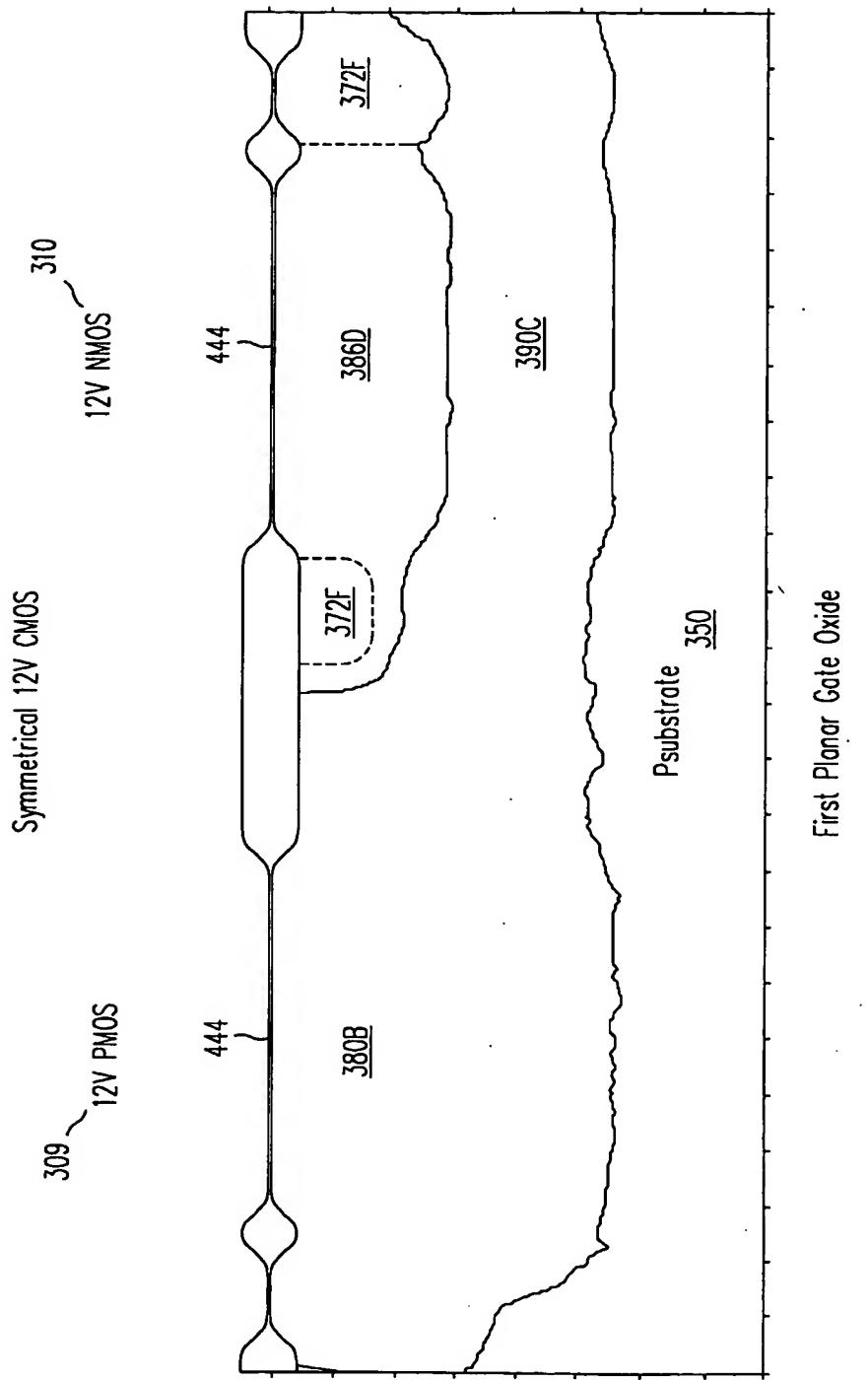


FIG. 47D



First Planar Gate Oxide

FIG. 48A



First Planar Gate Oxide

FIG. 48E

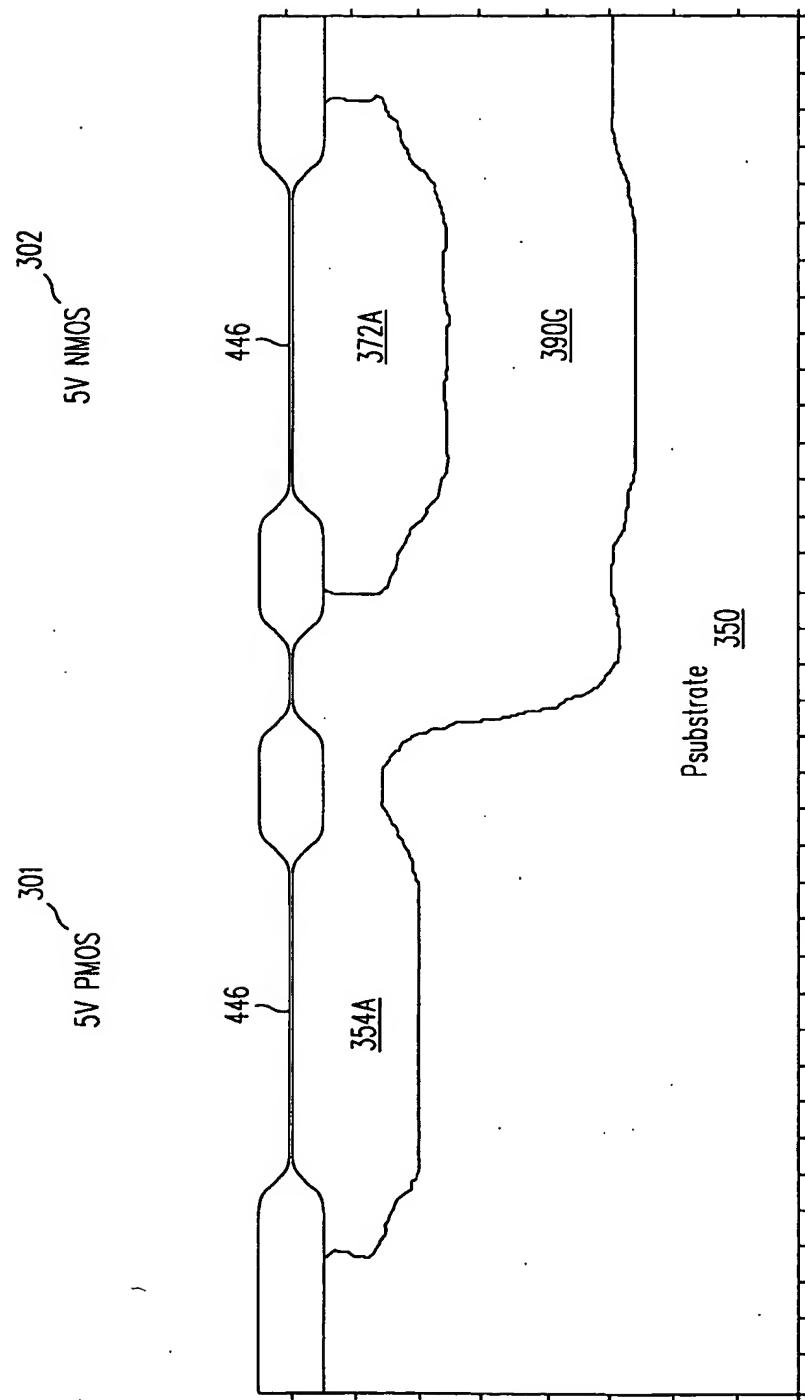


FIG. 49A

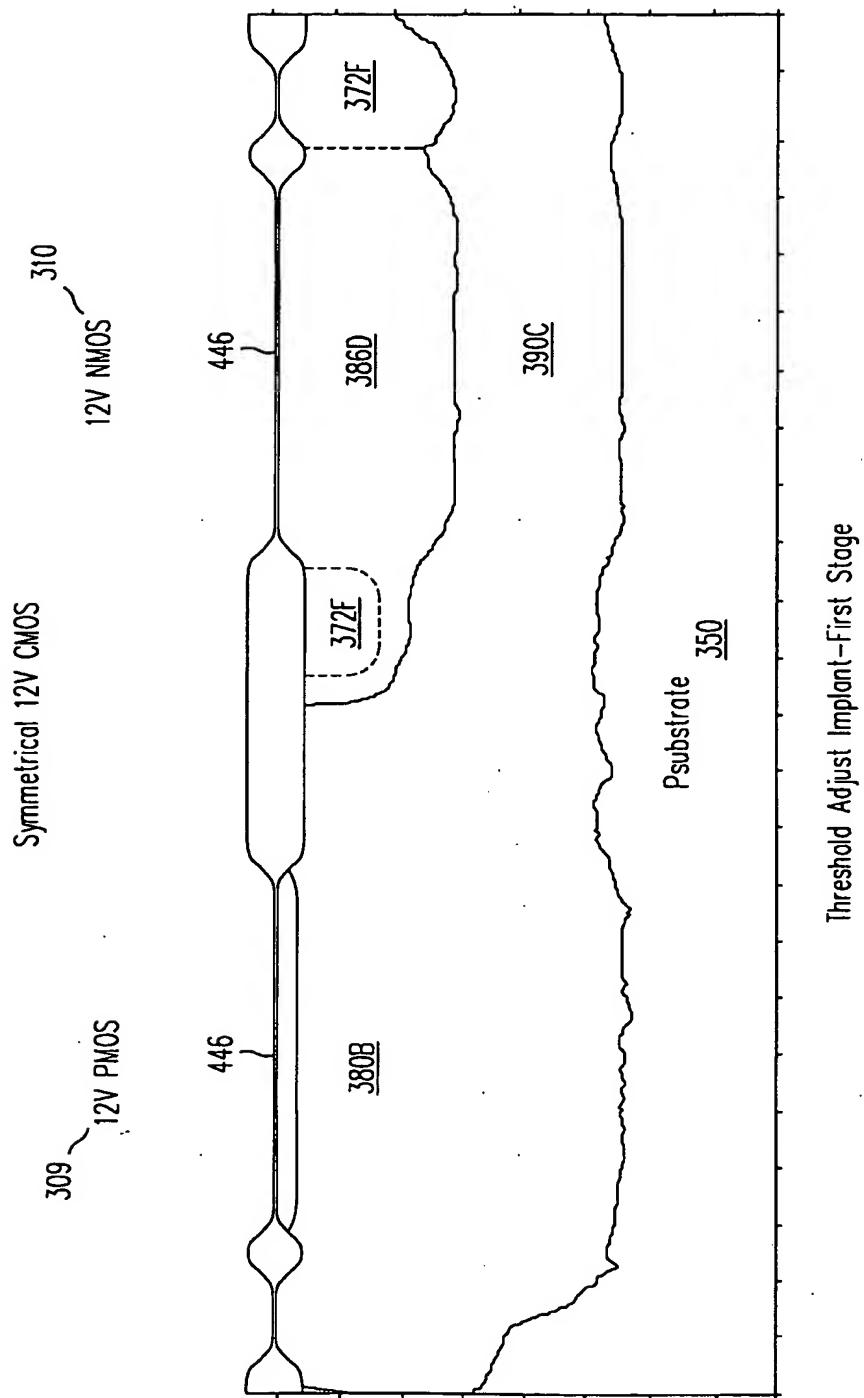
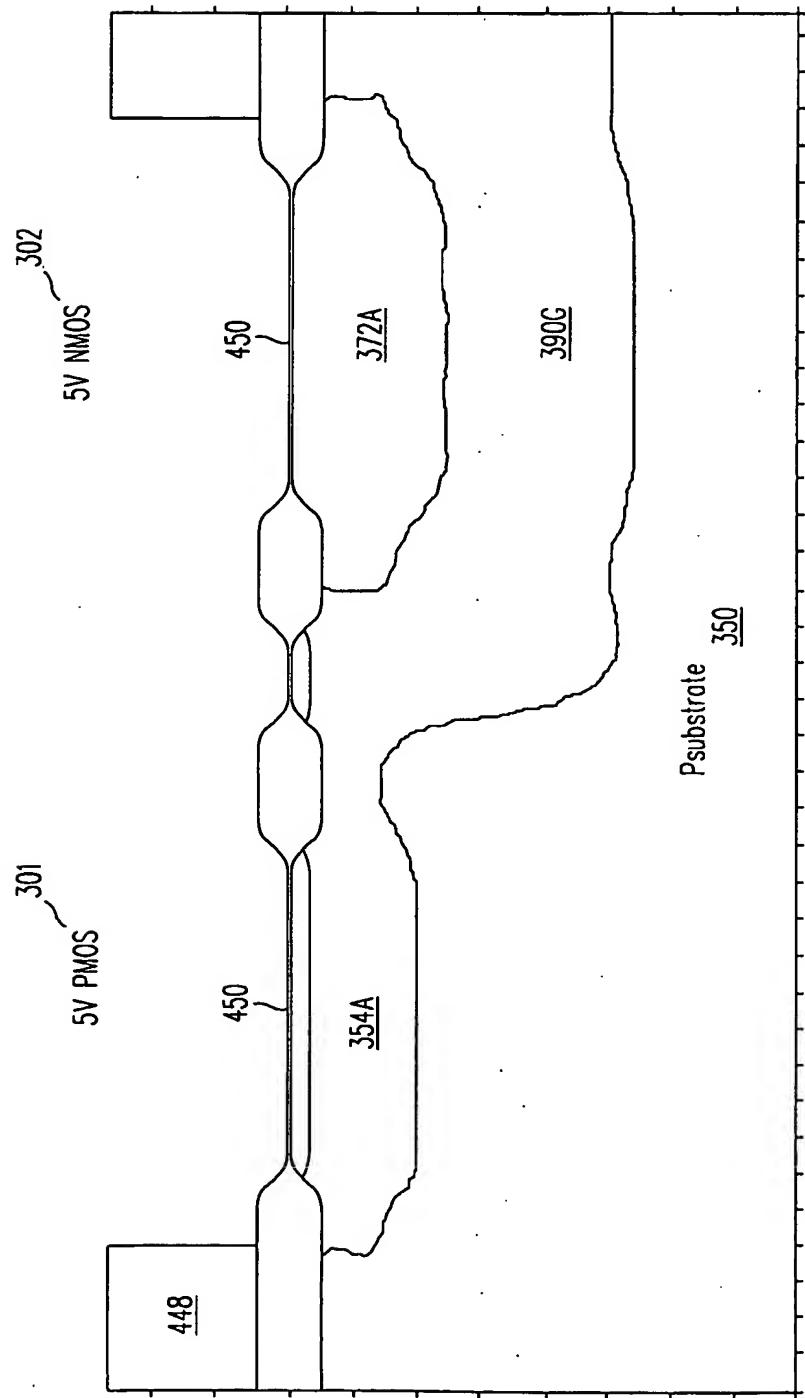


FIG. 49E



Threshold Adjust Implant-Second Stage
First Planar Gate Oxide Removal

FIG. 50A

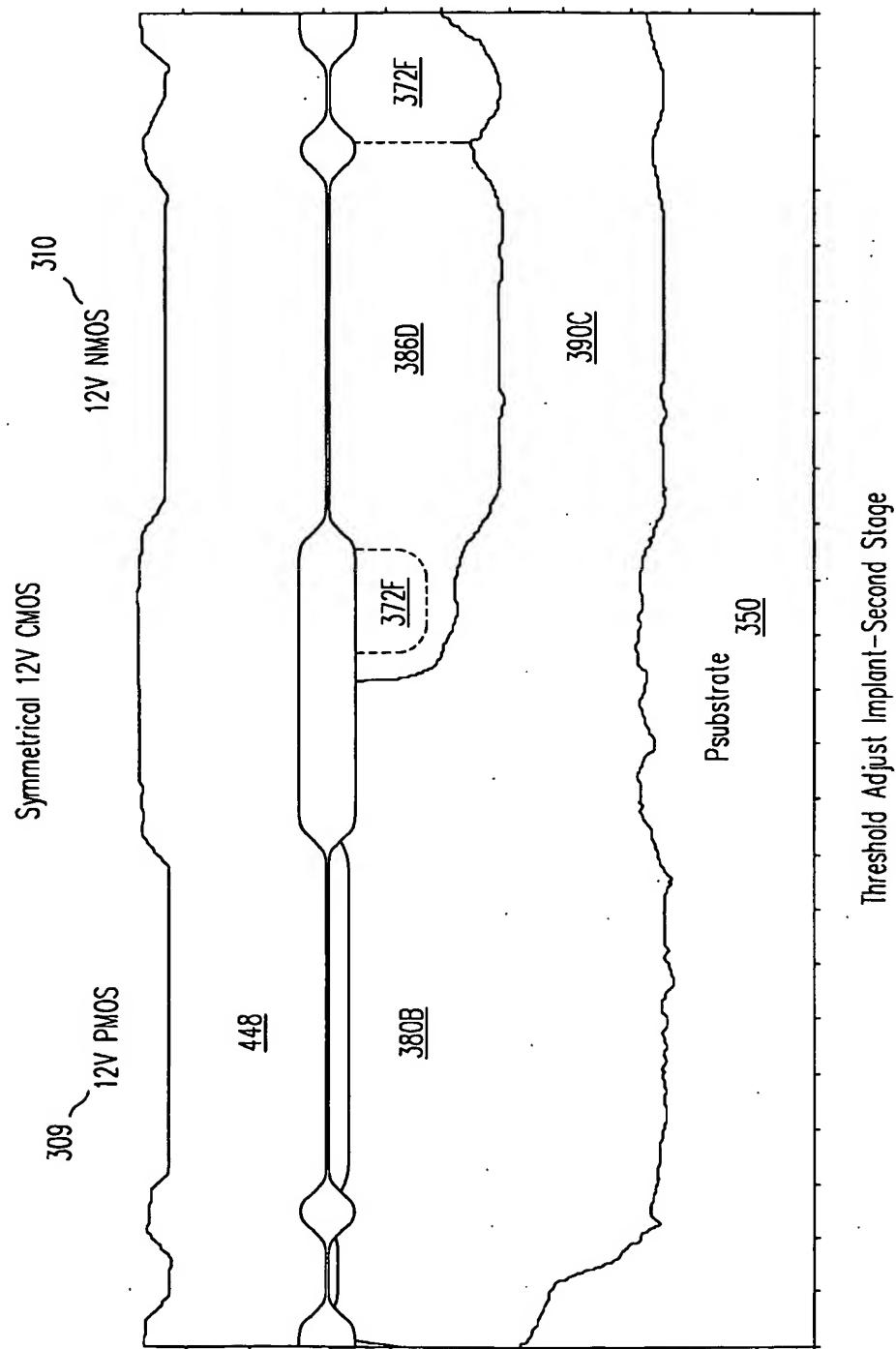


FIG. 50E

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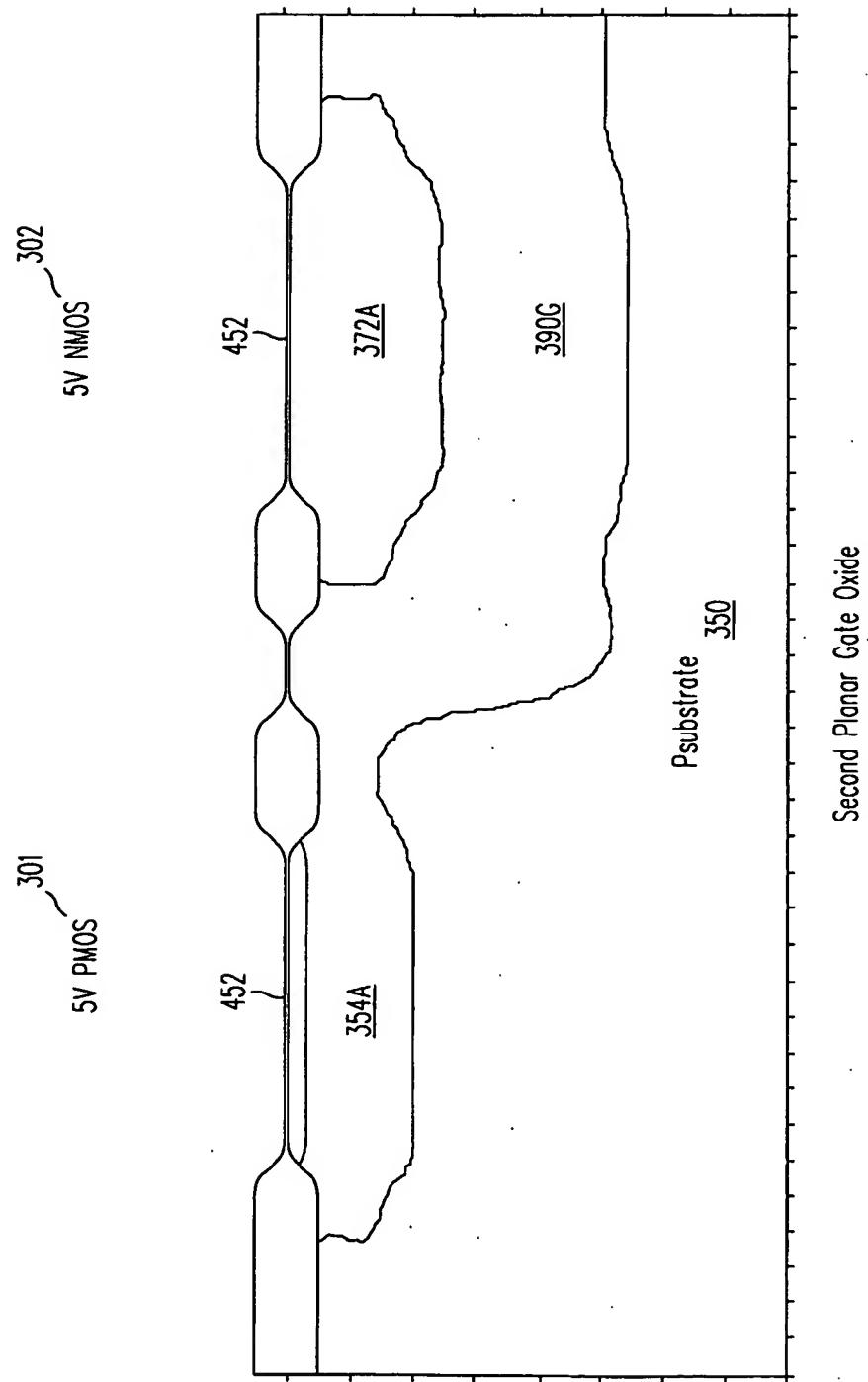
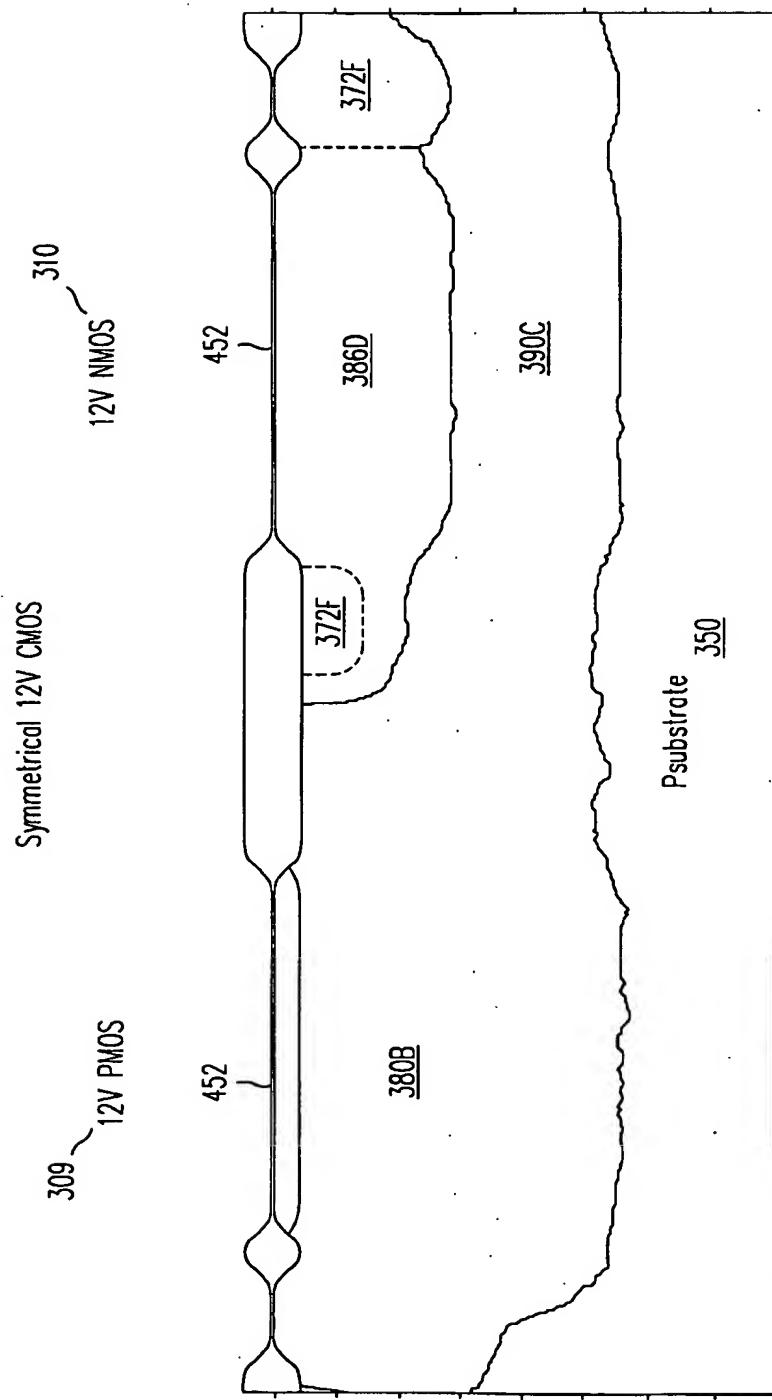
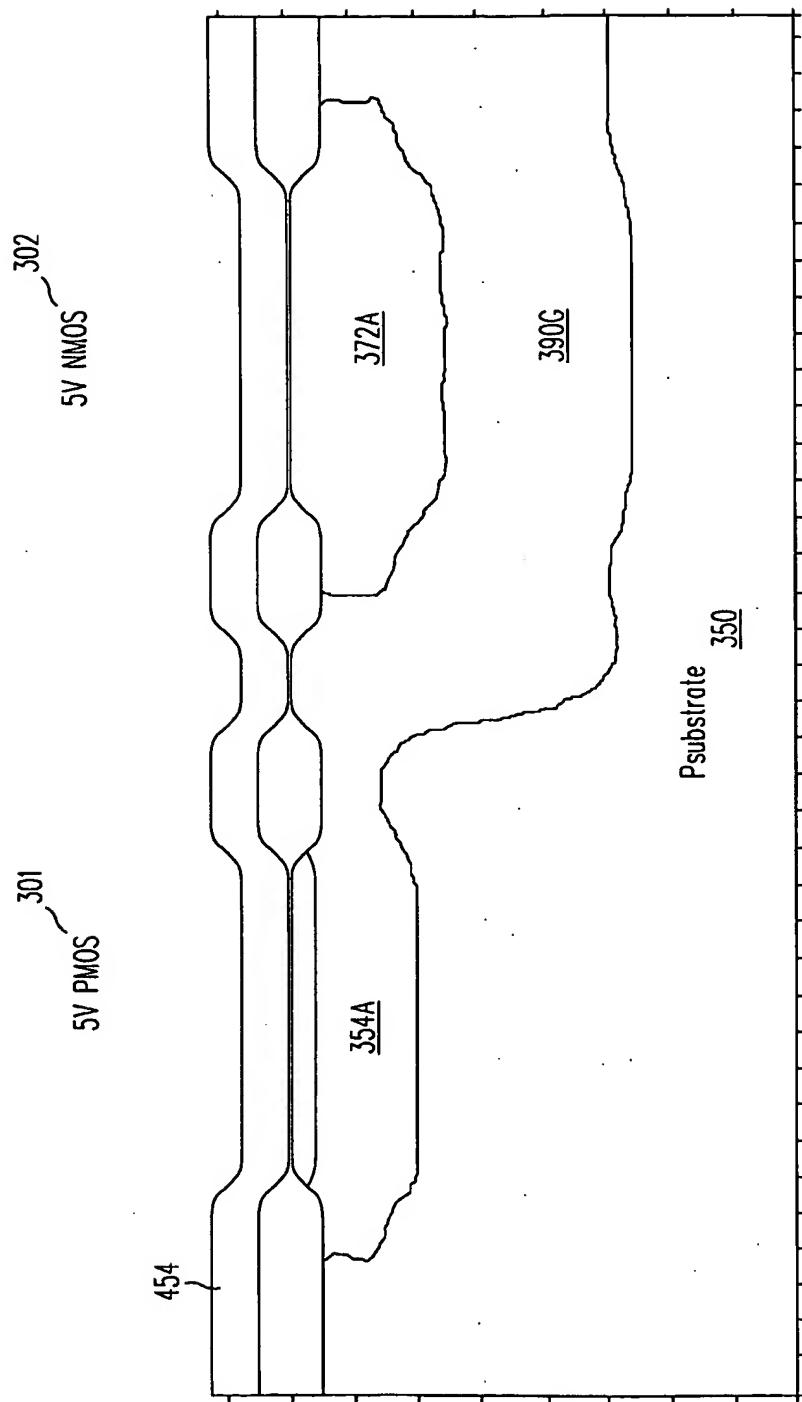


FIG. 51A



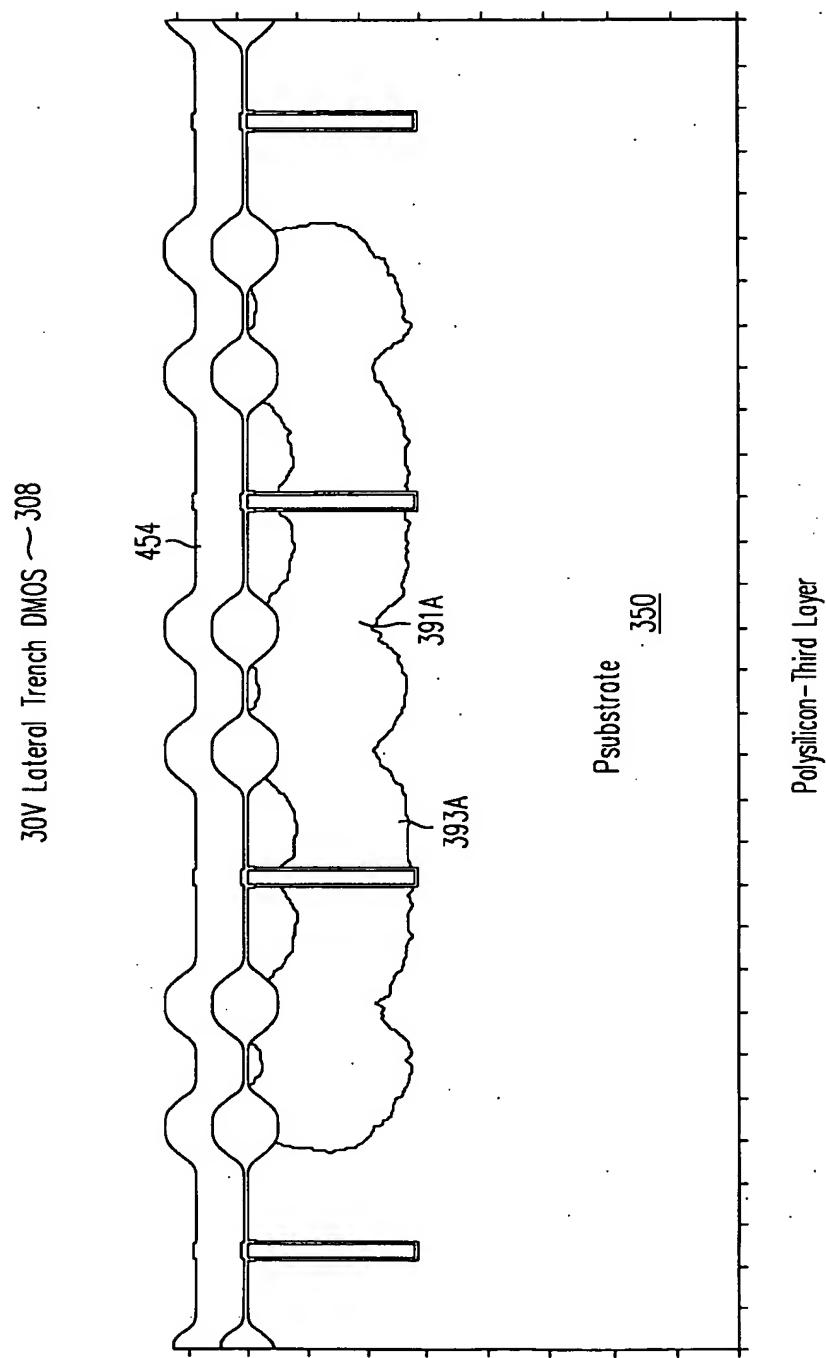
Second Planar Gate Oxide

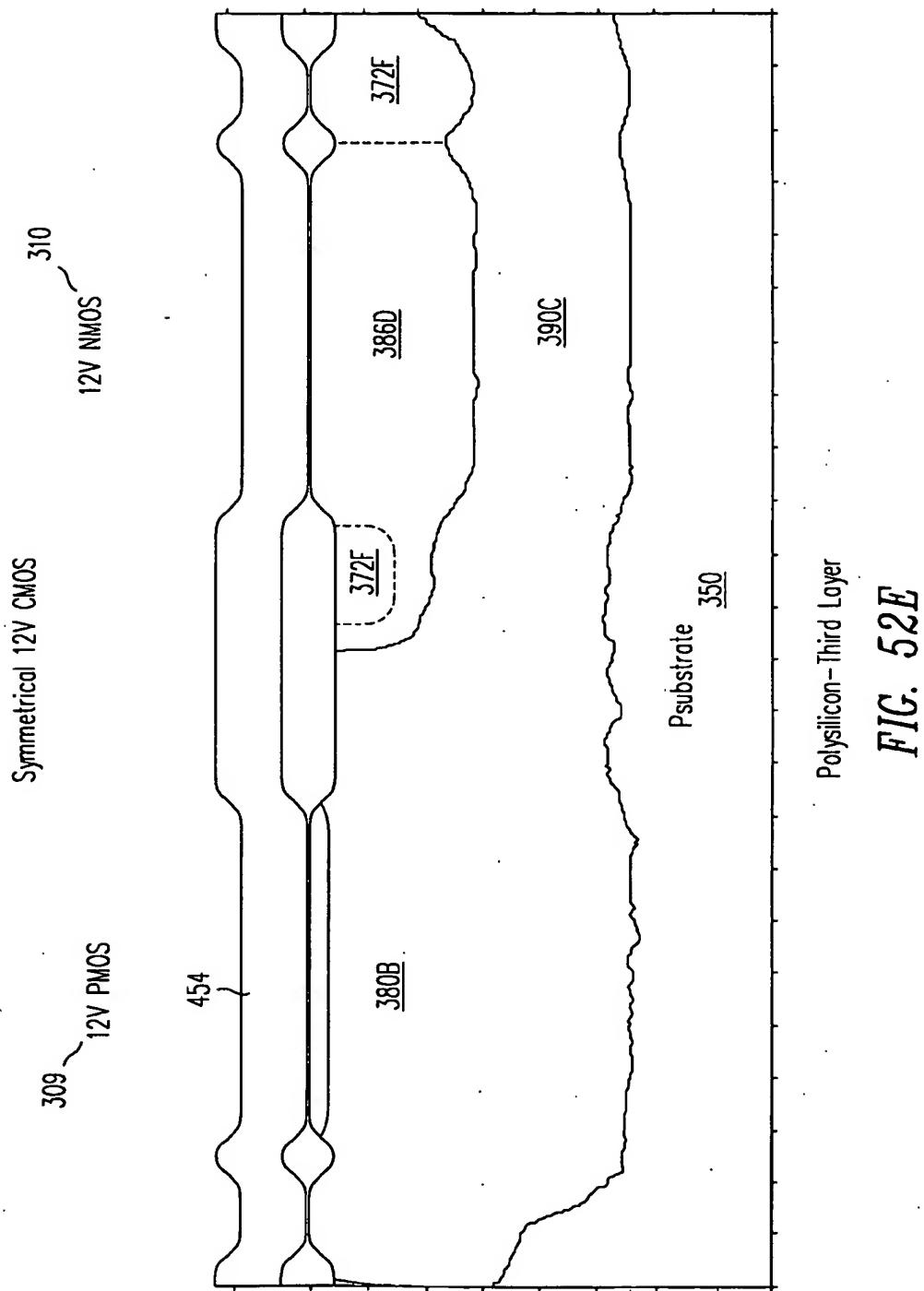
FIG. 51E



Polysilicon-Third Layer

FIG. 52A





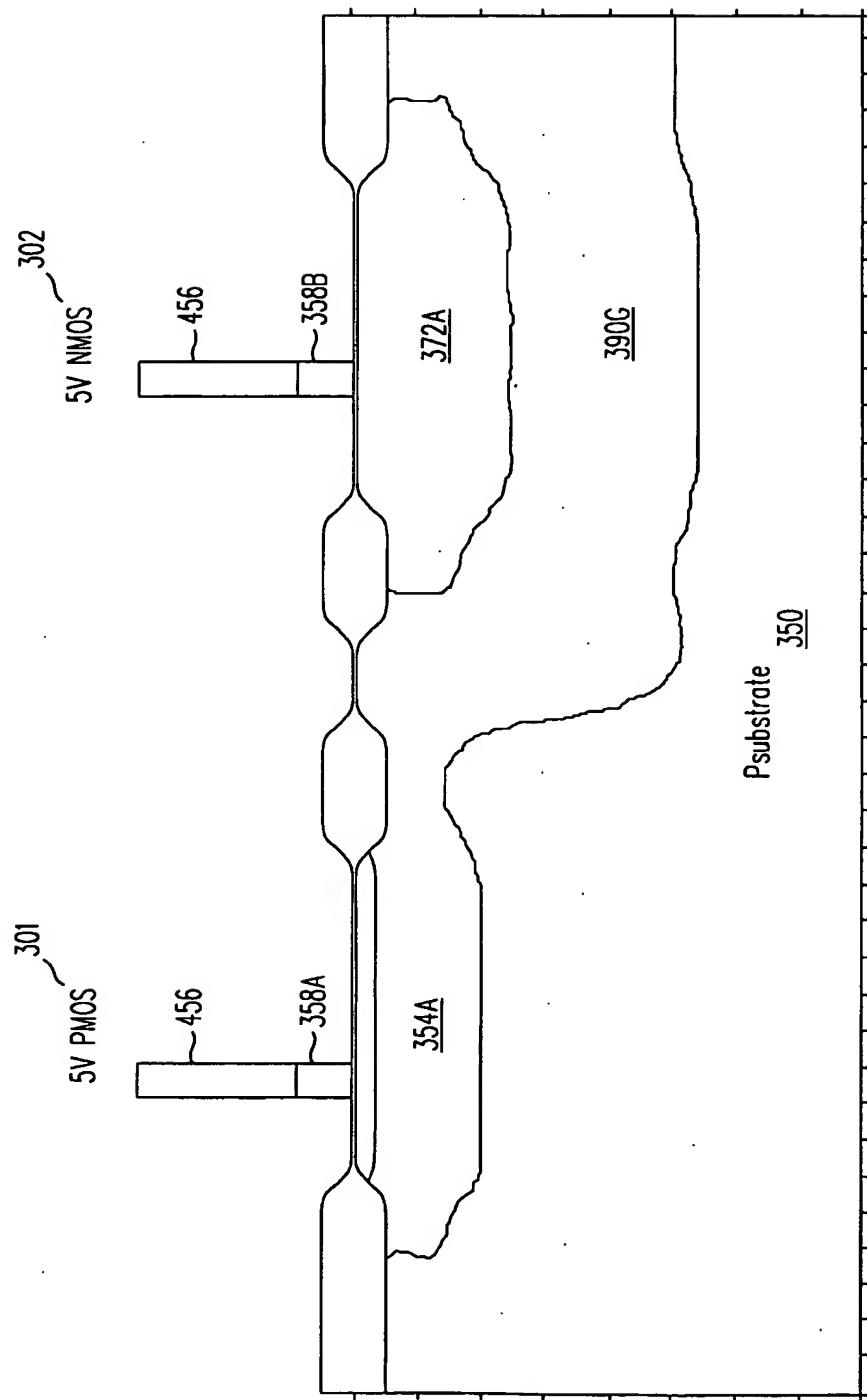
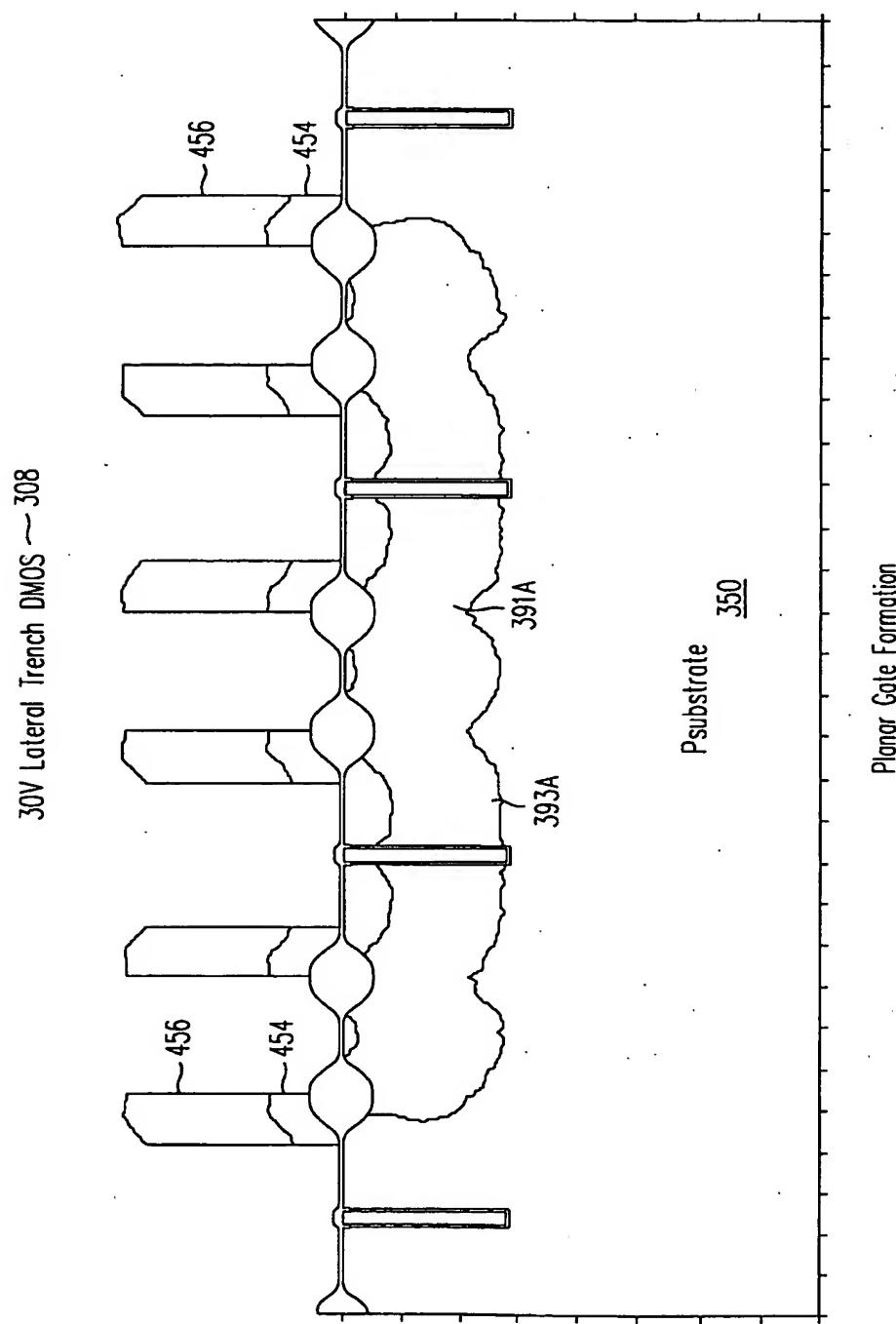


FIG. 53A



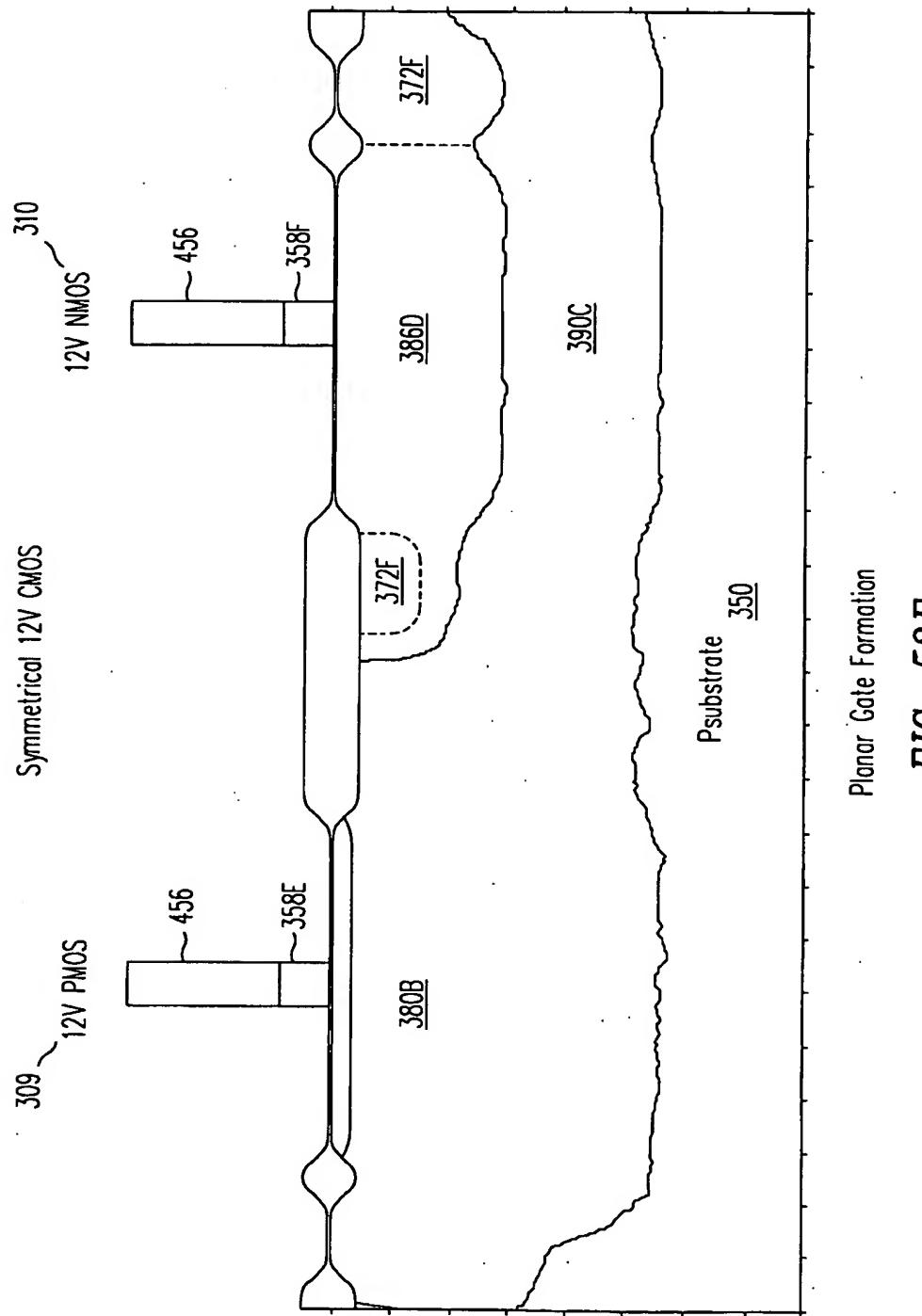
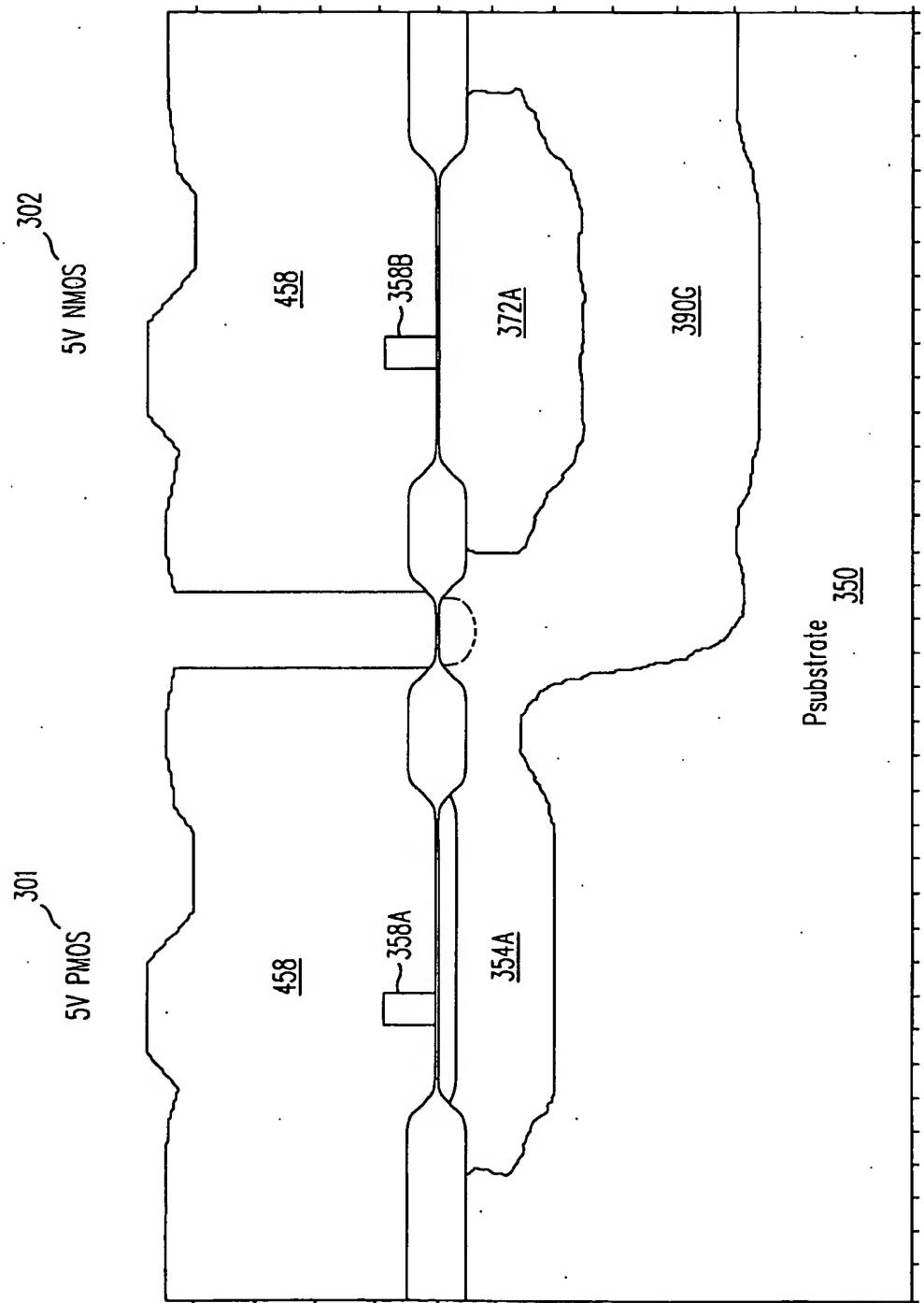


FIG. 53E



N-Base Mask and Implant

FIG. 54A

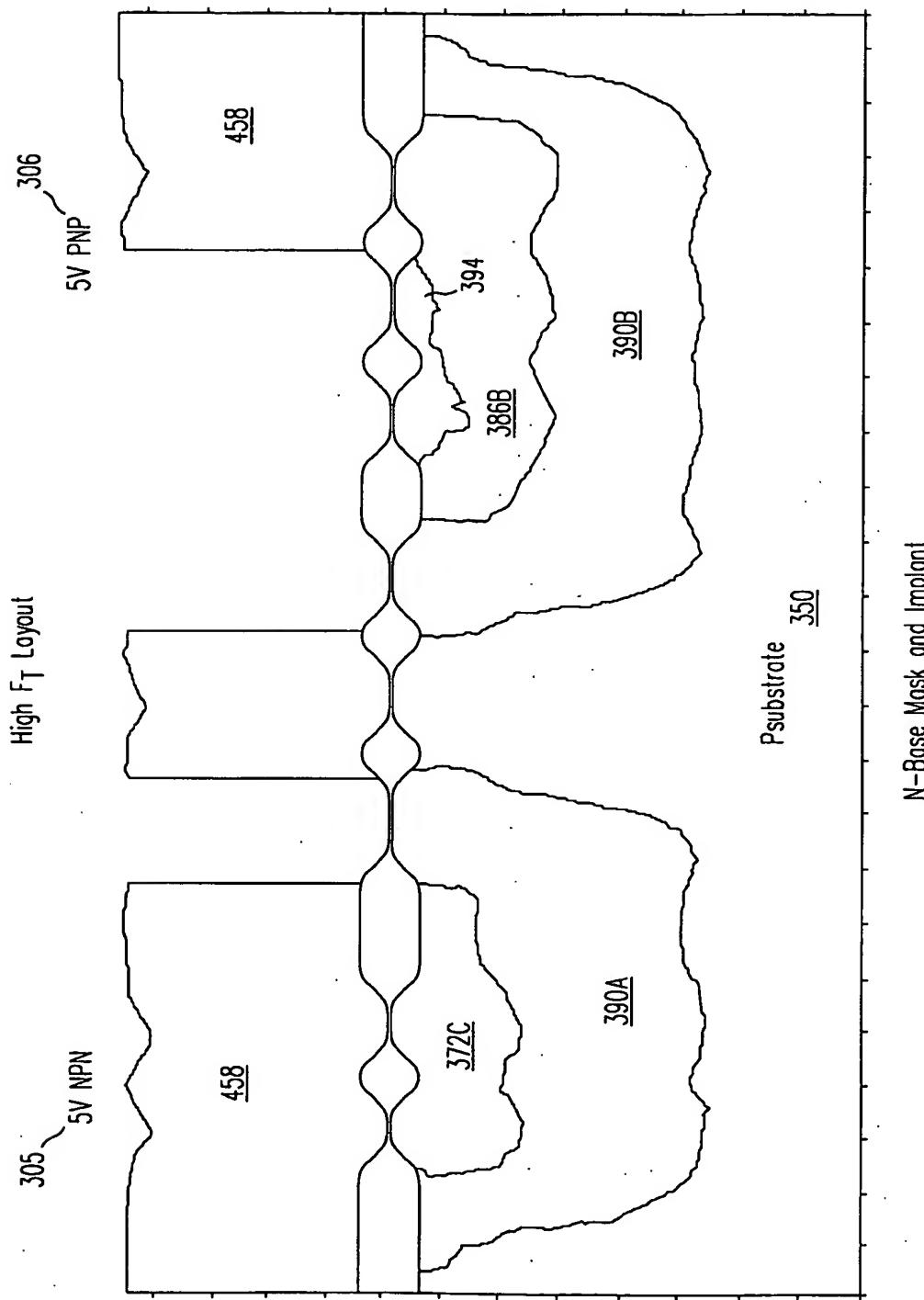


FIG. 54B

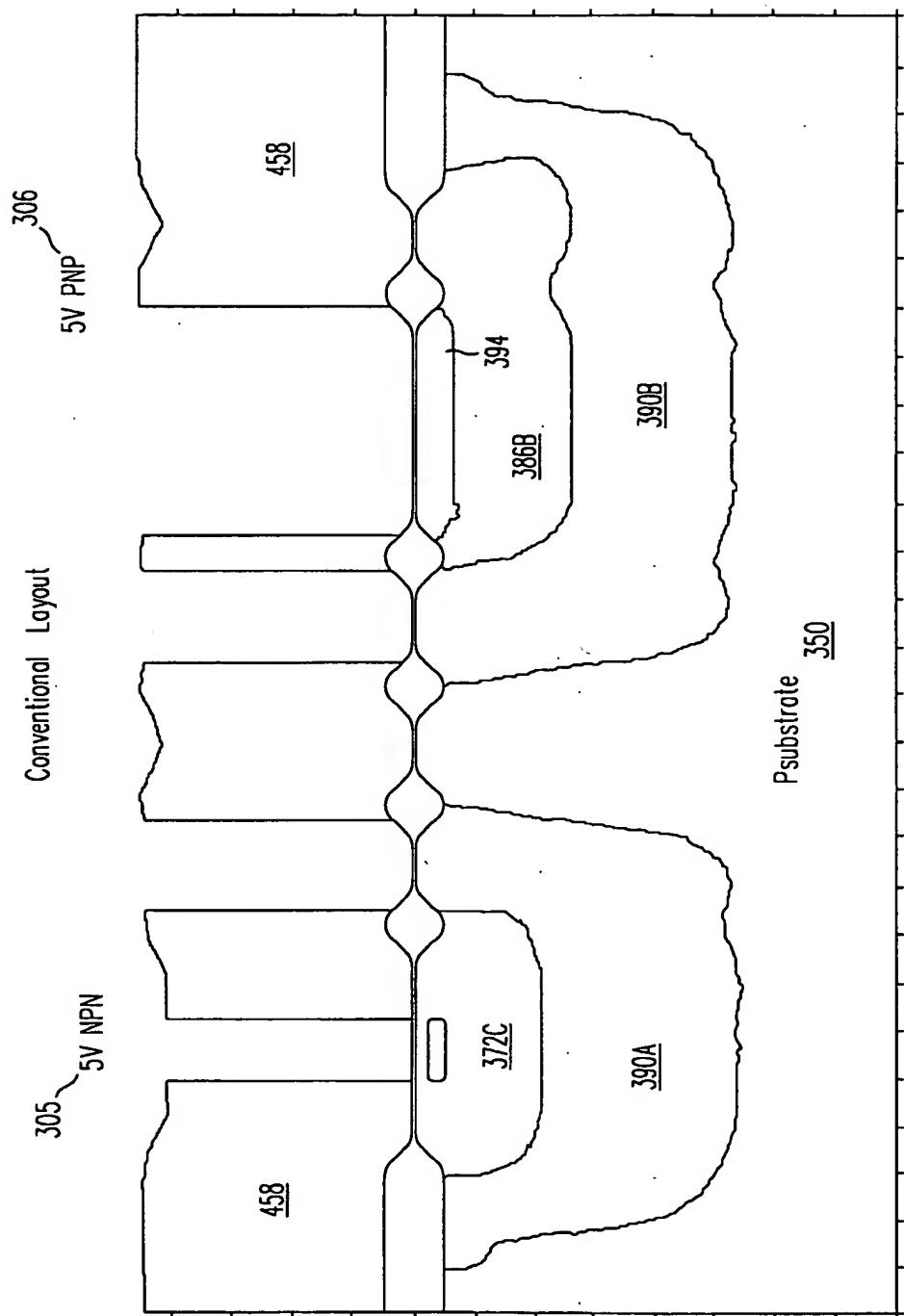
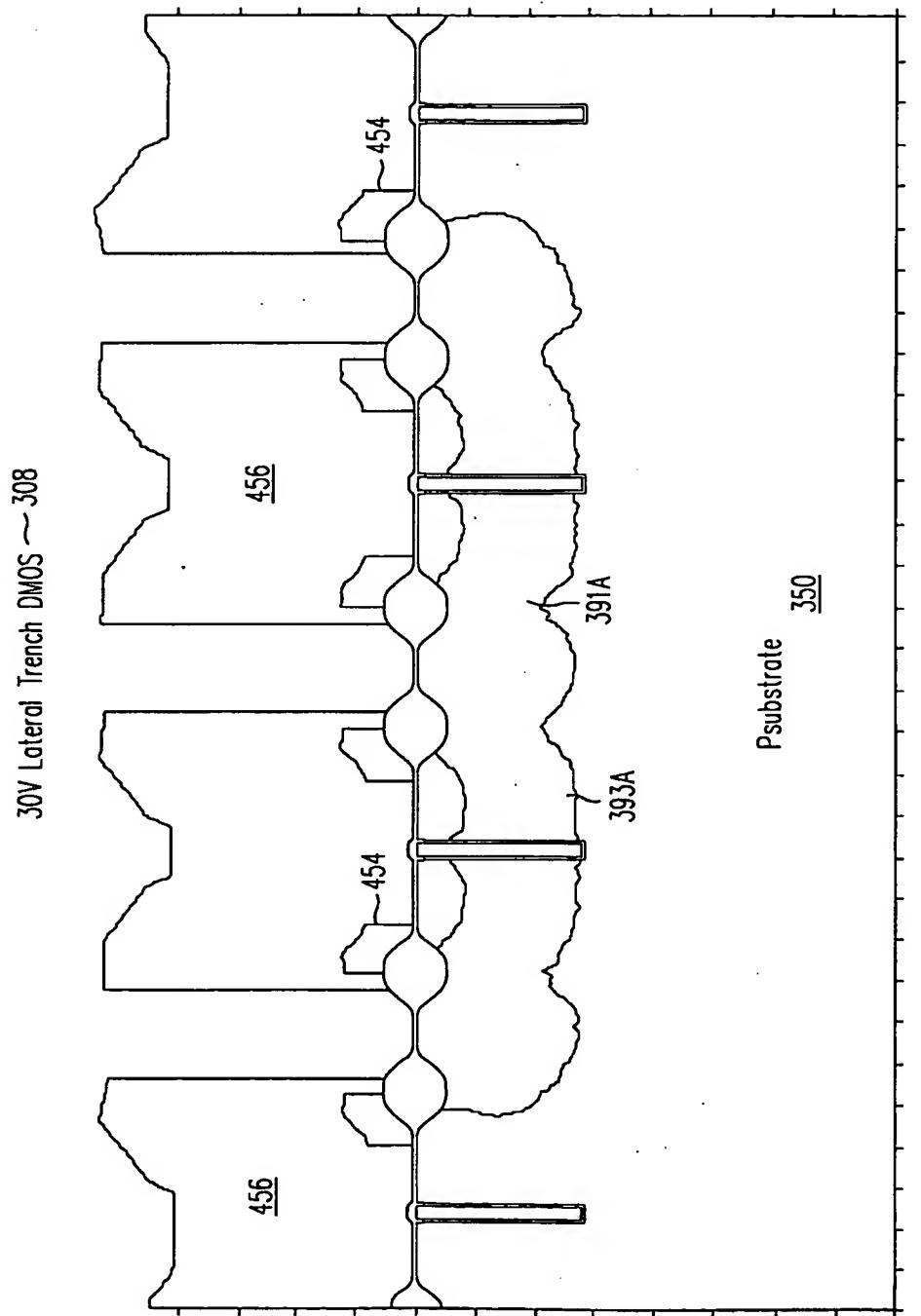
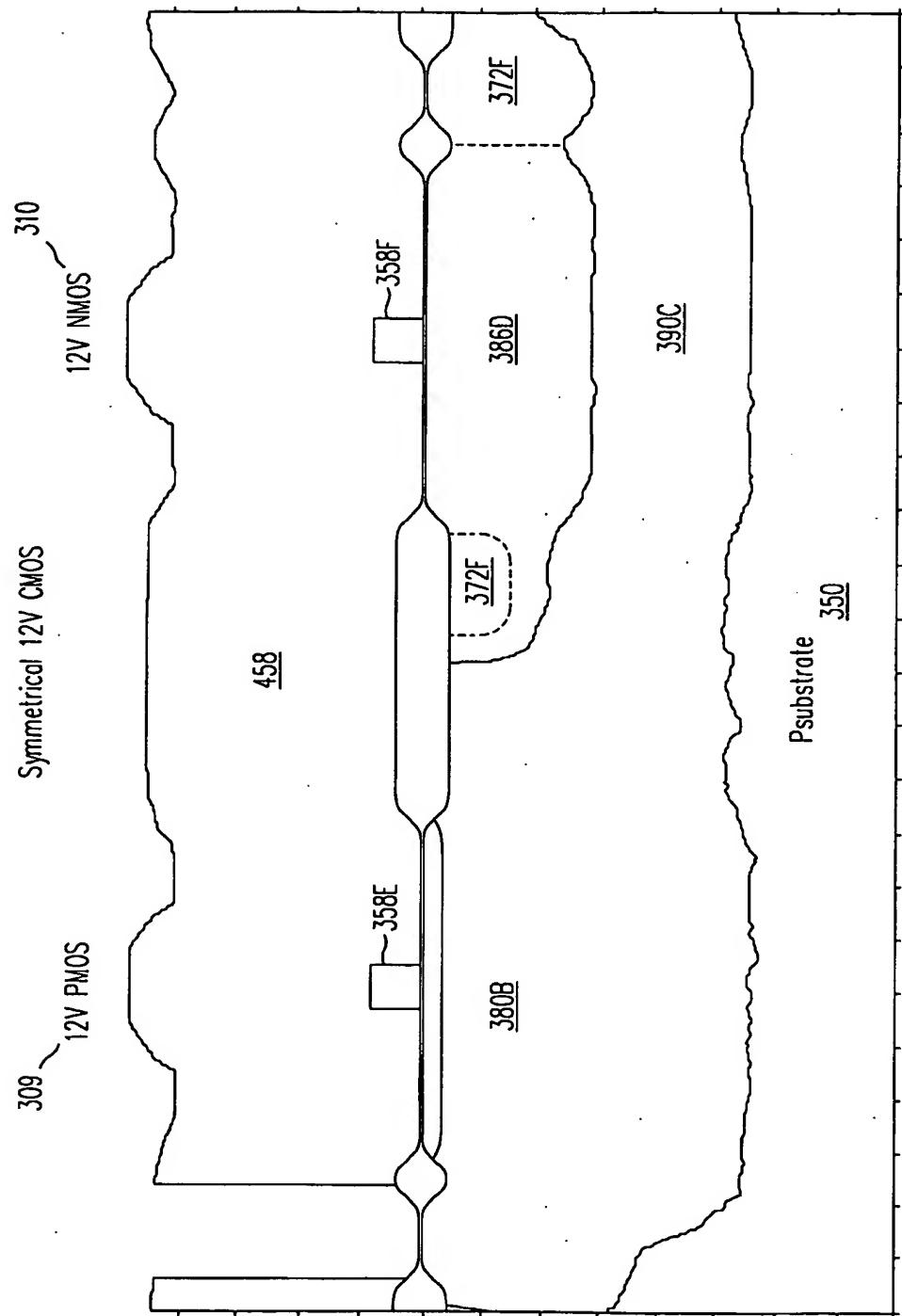


FIG. 54C



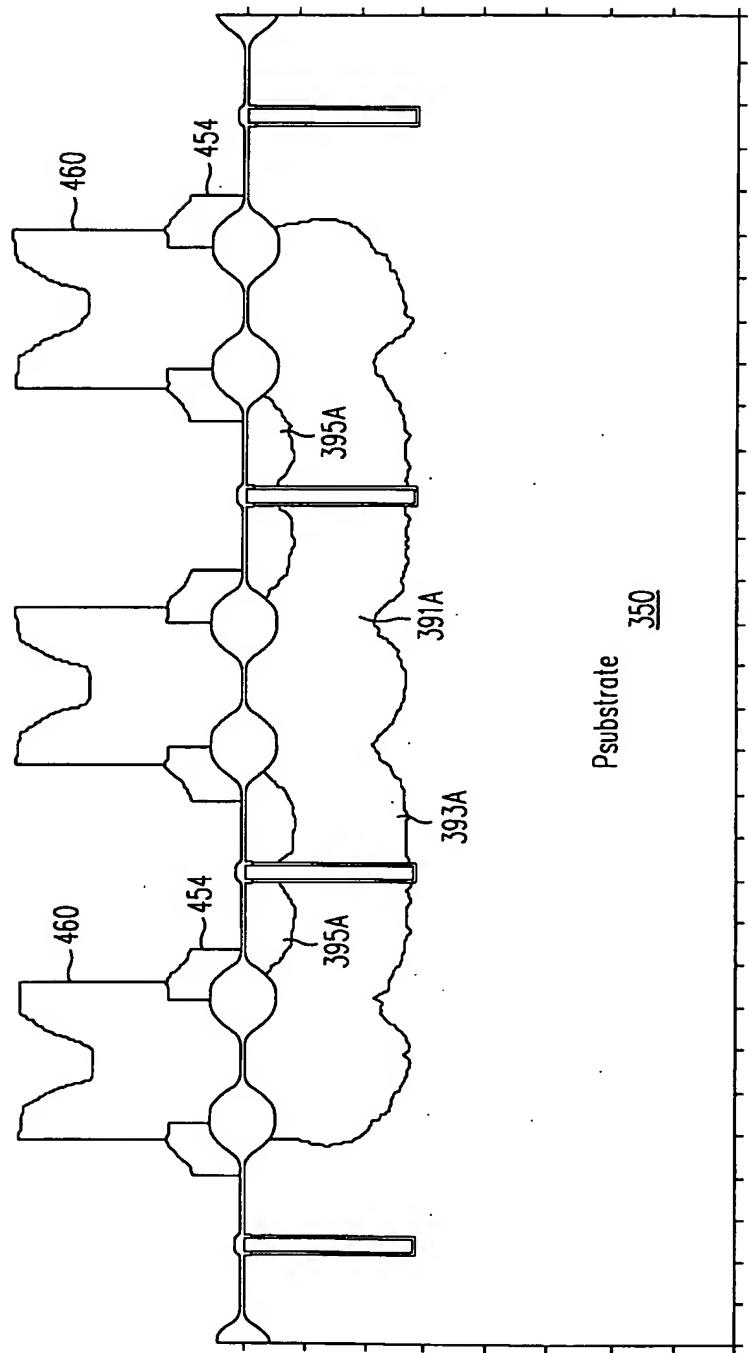
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N-Base Mask and Implant

FIG. 54E

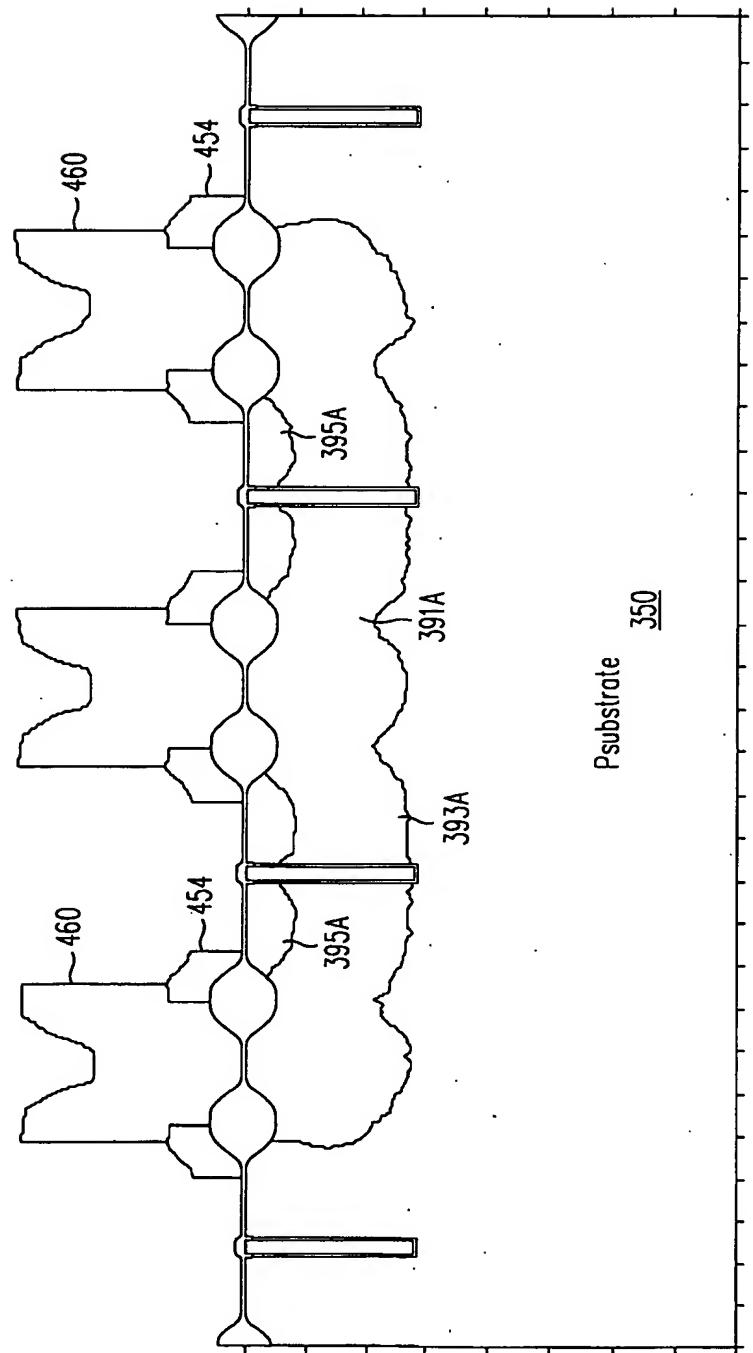
30V Lateral Trench DMOS ~ 308



P Body Mask and Implant-First Stage

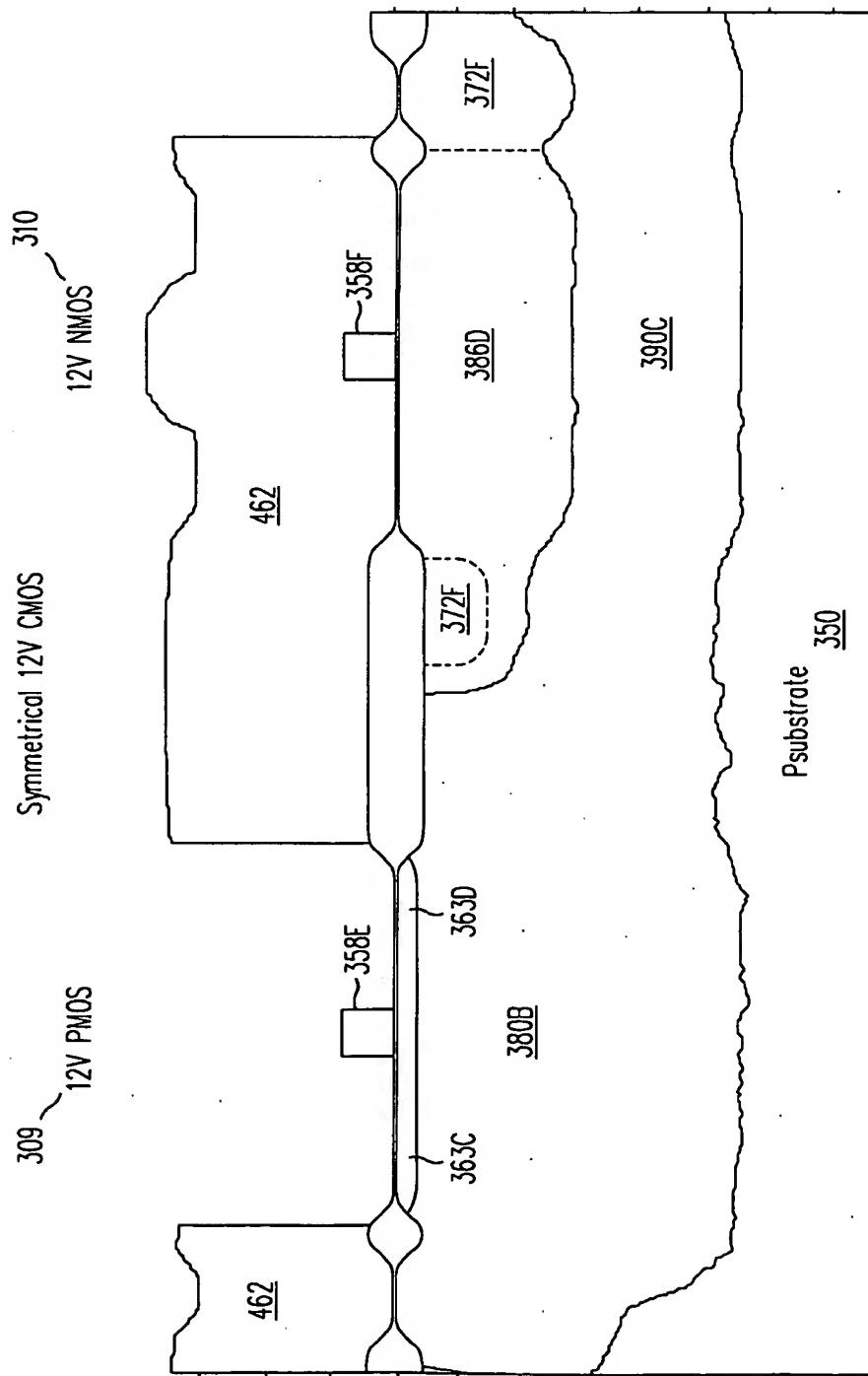
FIG. 55D

30V Lateral trench DMOS — 308



P Body Mask and Implant-Second Stage

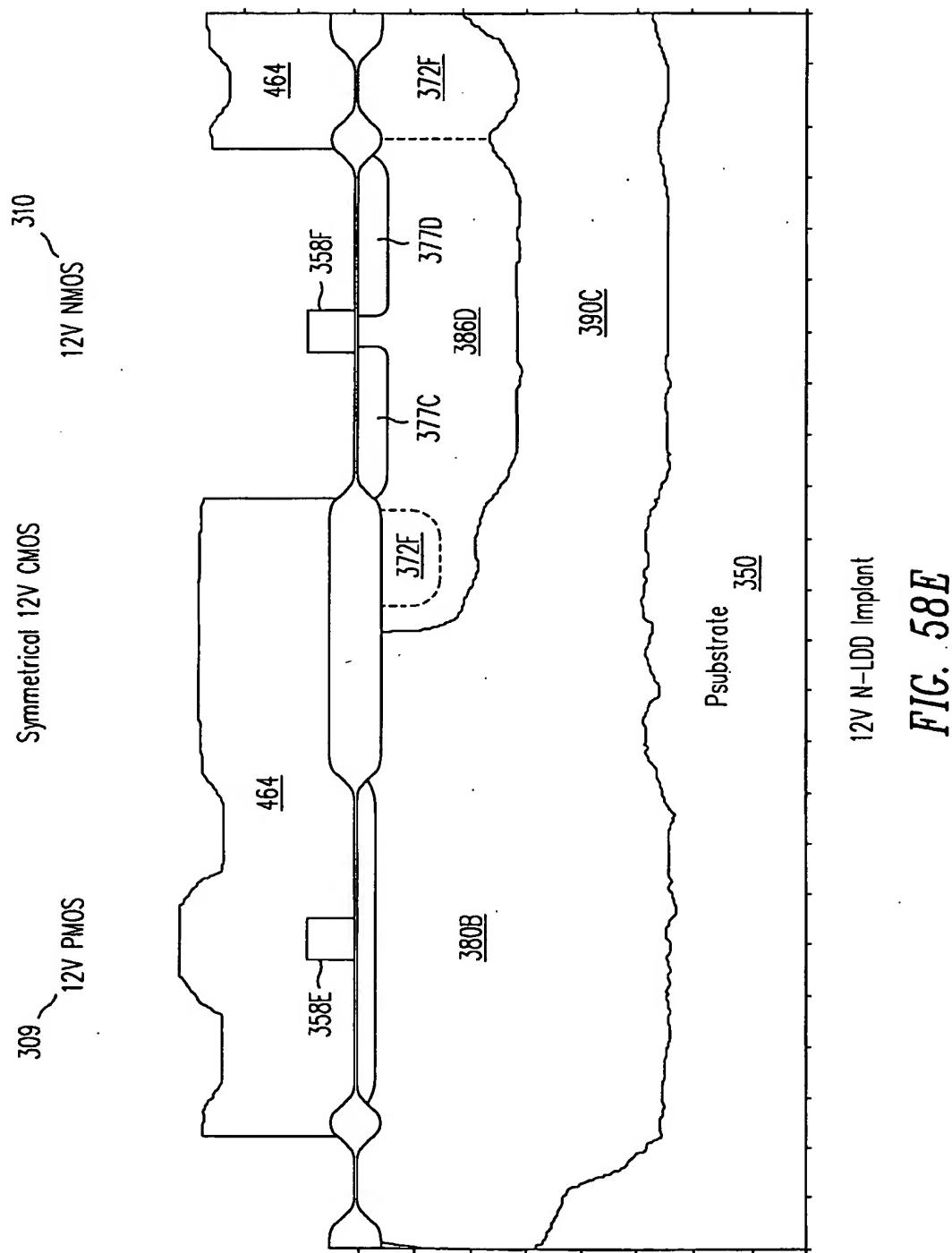
FIG. 56D



12V P-LDD implant

FIG. 57E

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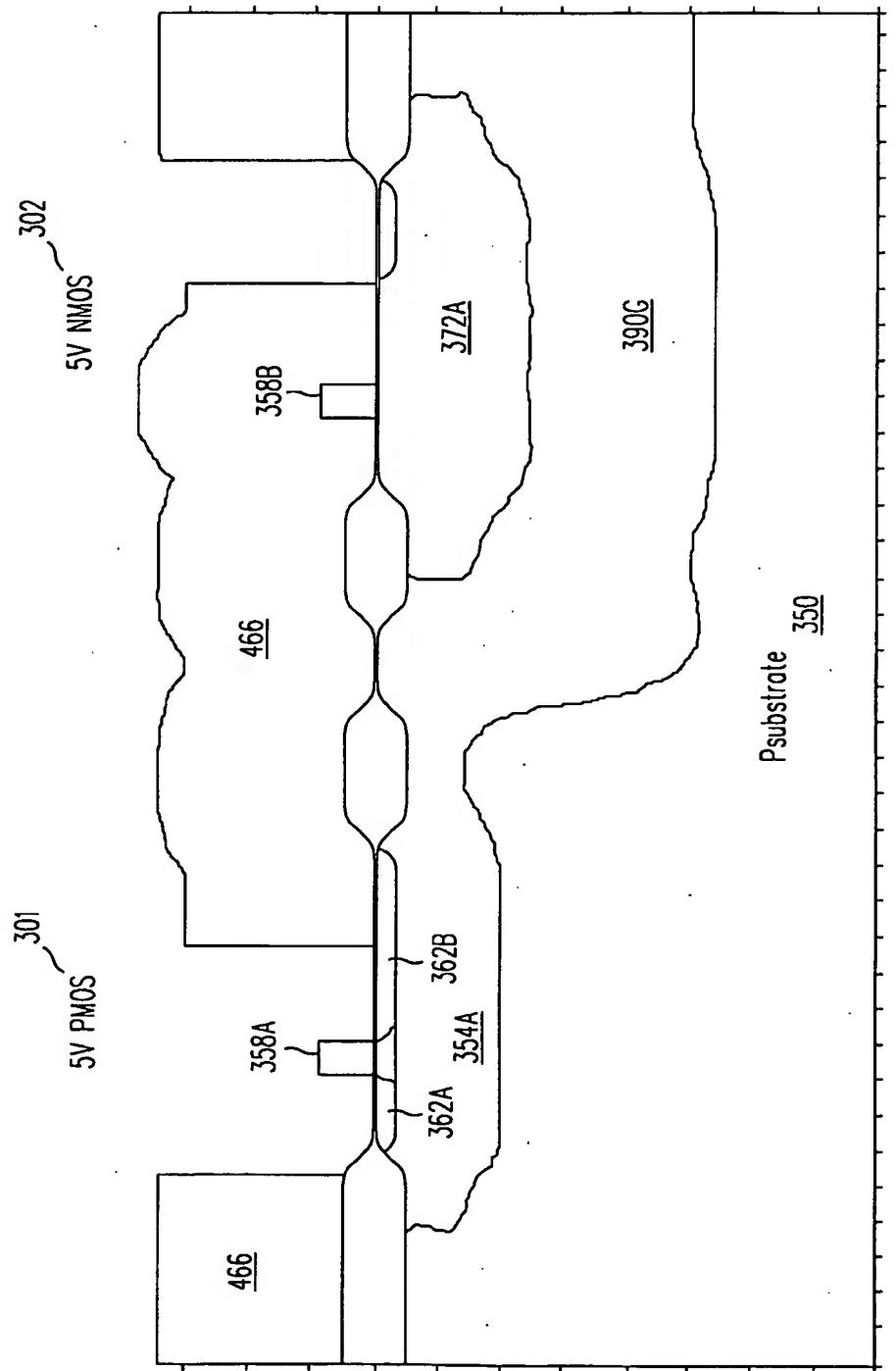


FIG. 59A

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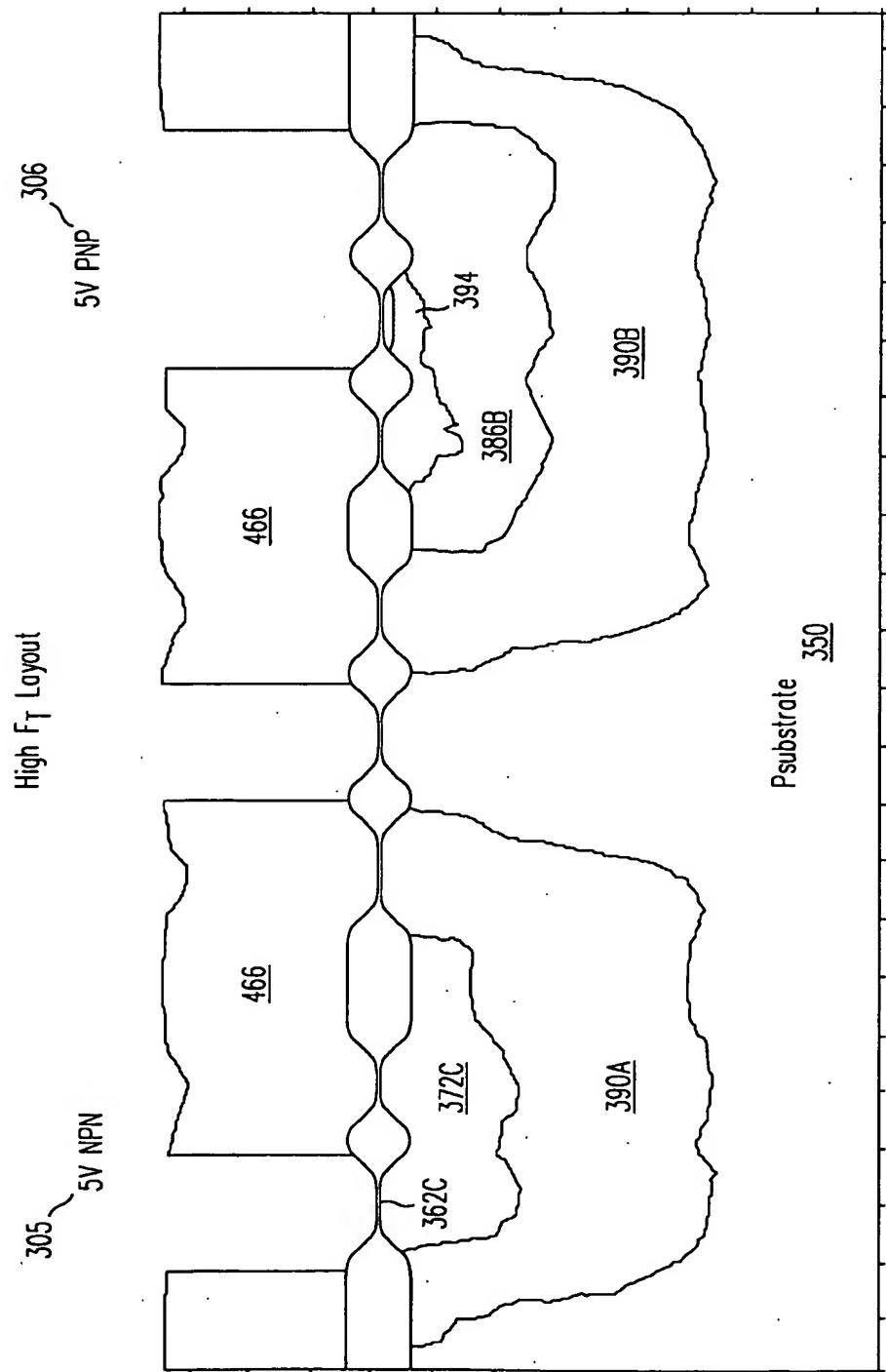
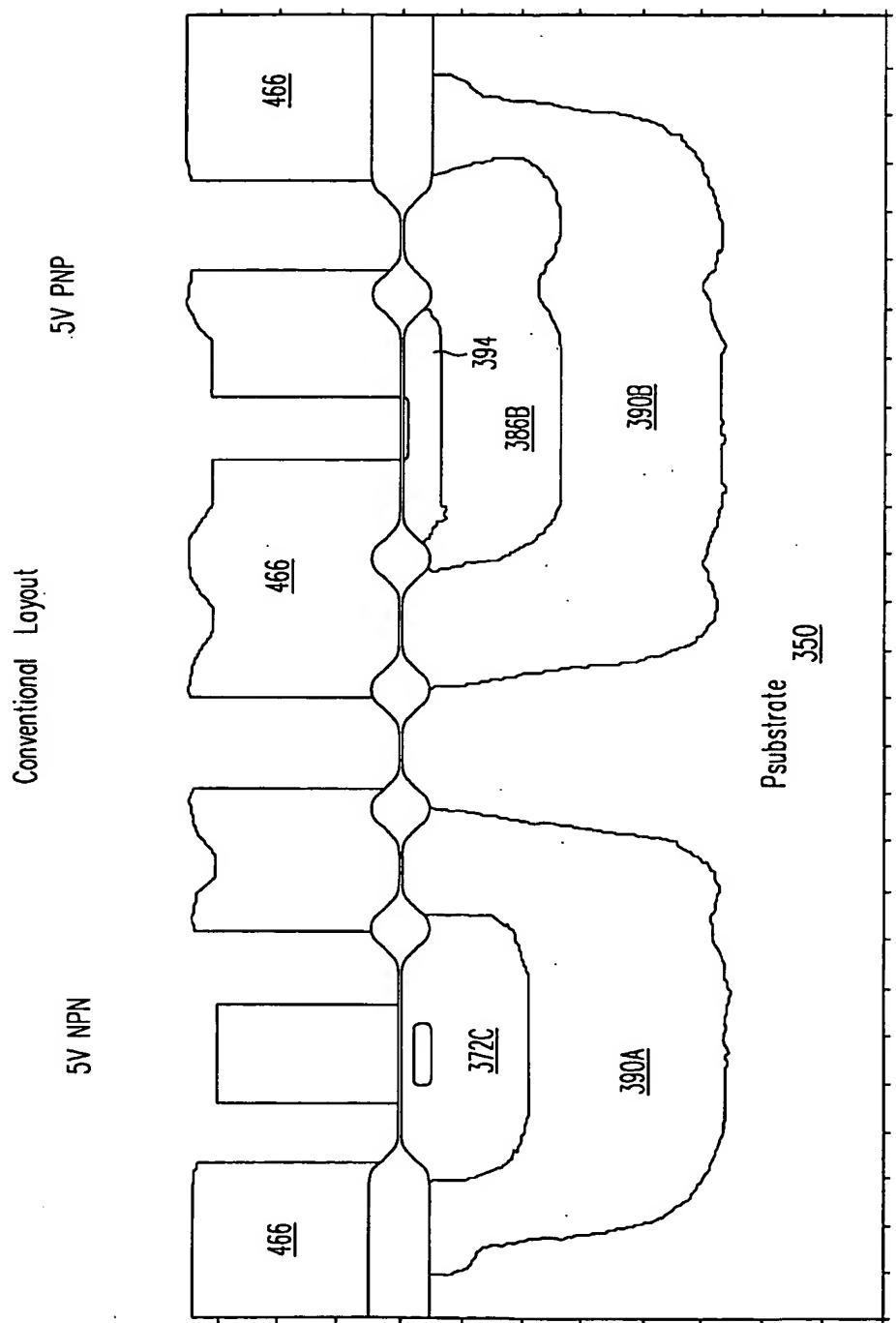
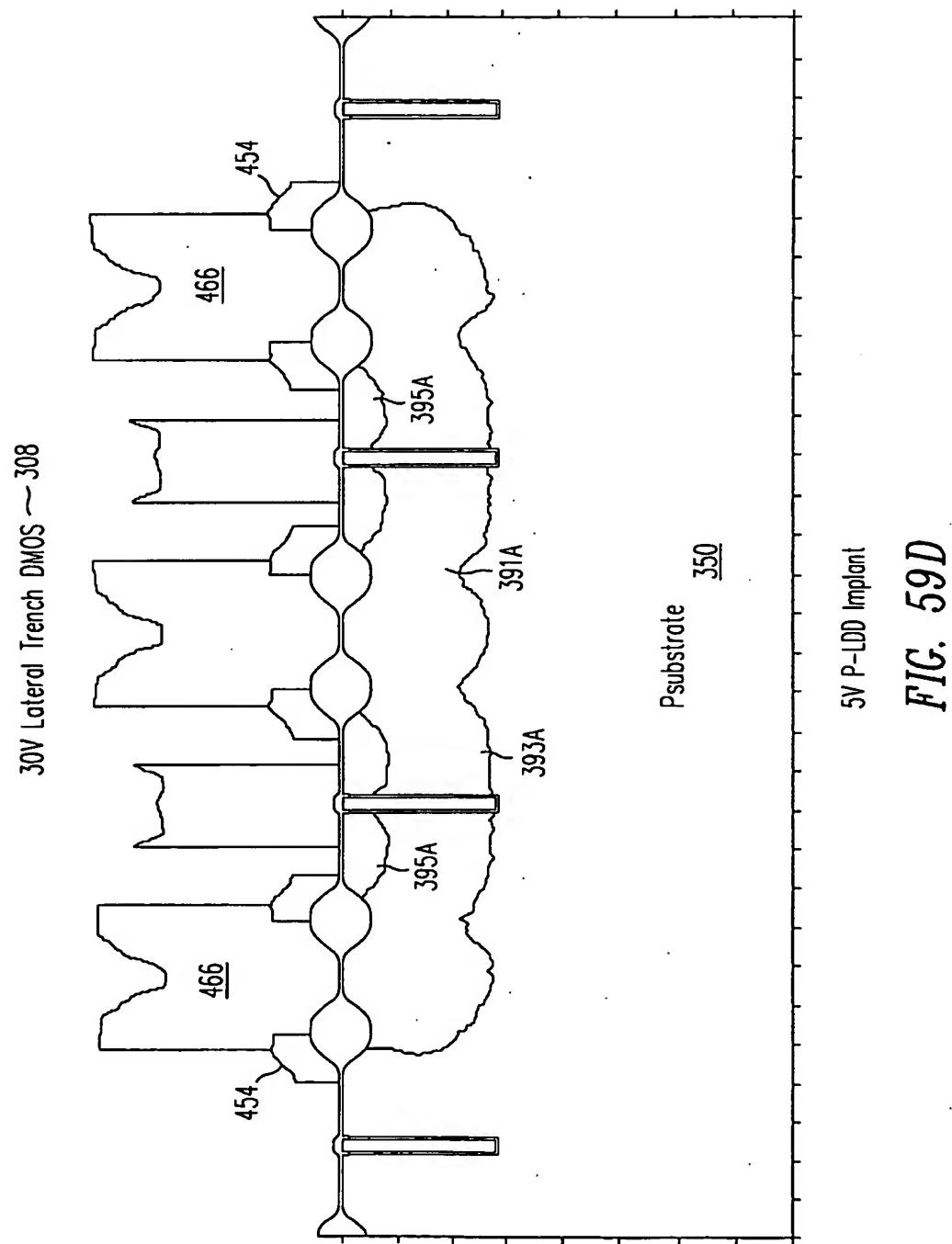
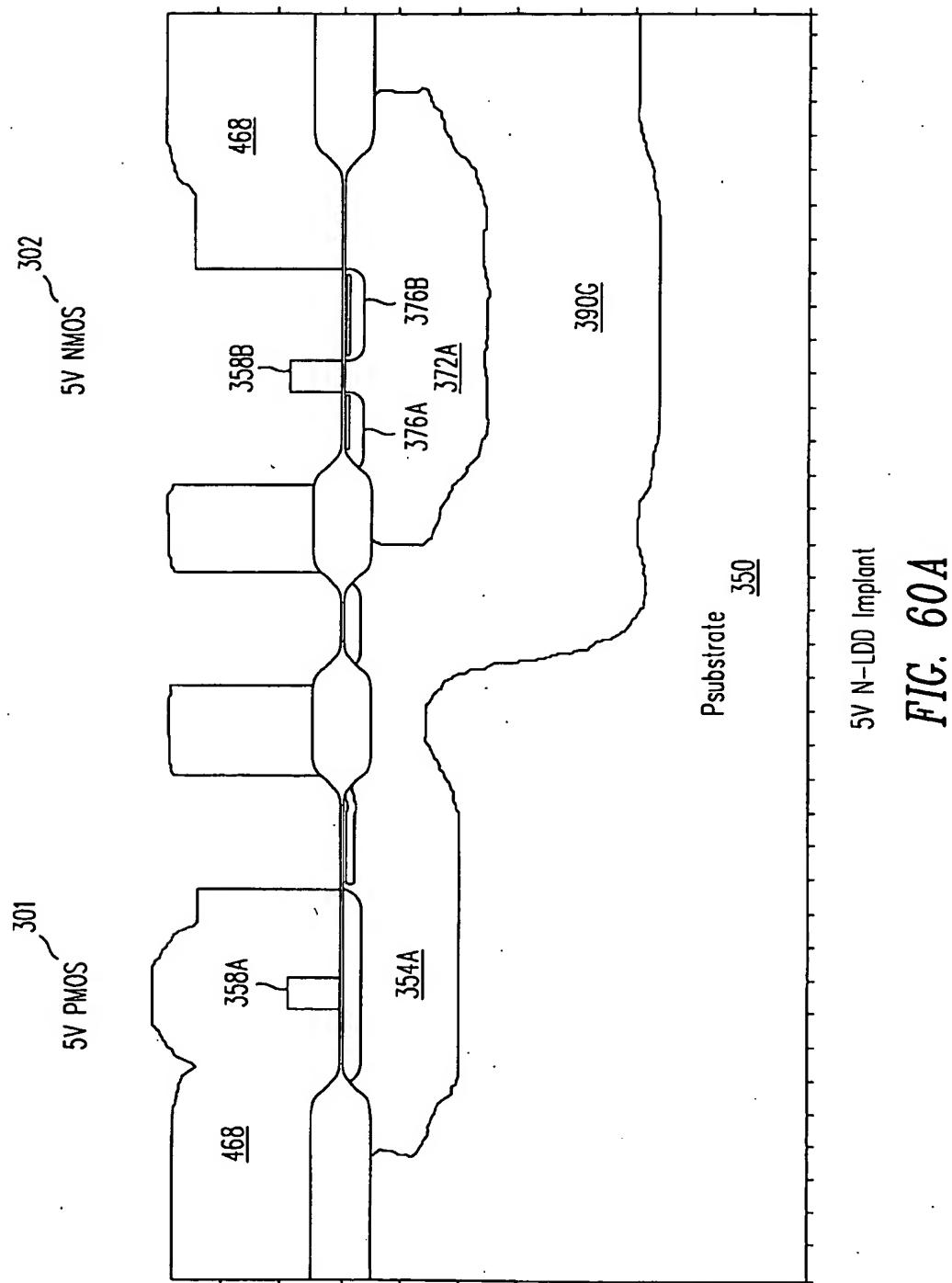


FIG. 59B



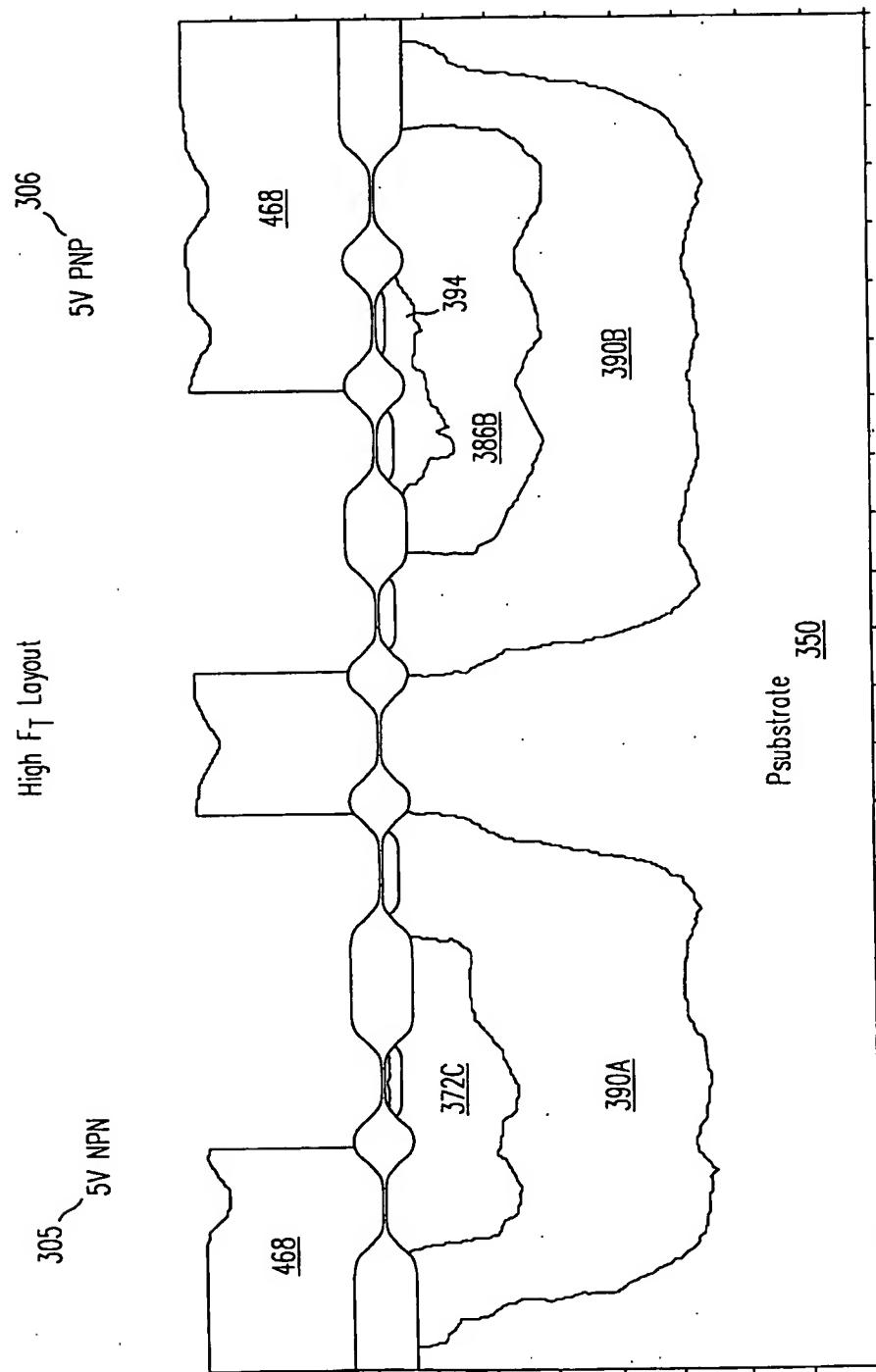
5V P-LOD Implant
FIG. 59C





5V N-LDD implant

FIG. 60A



5V N-LDD Implant
FIG. 60B

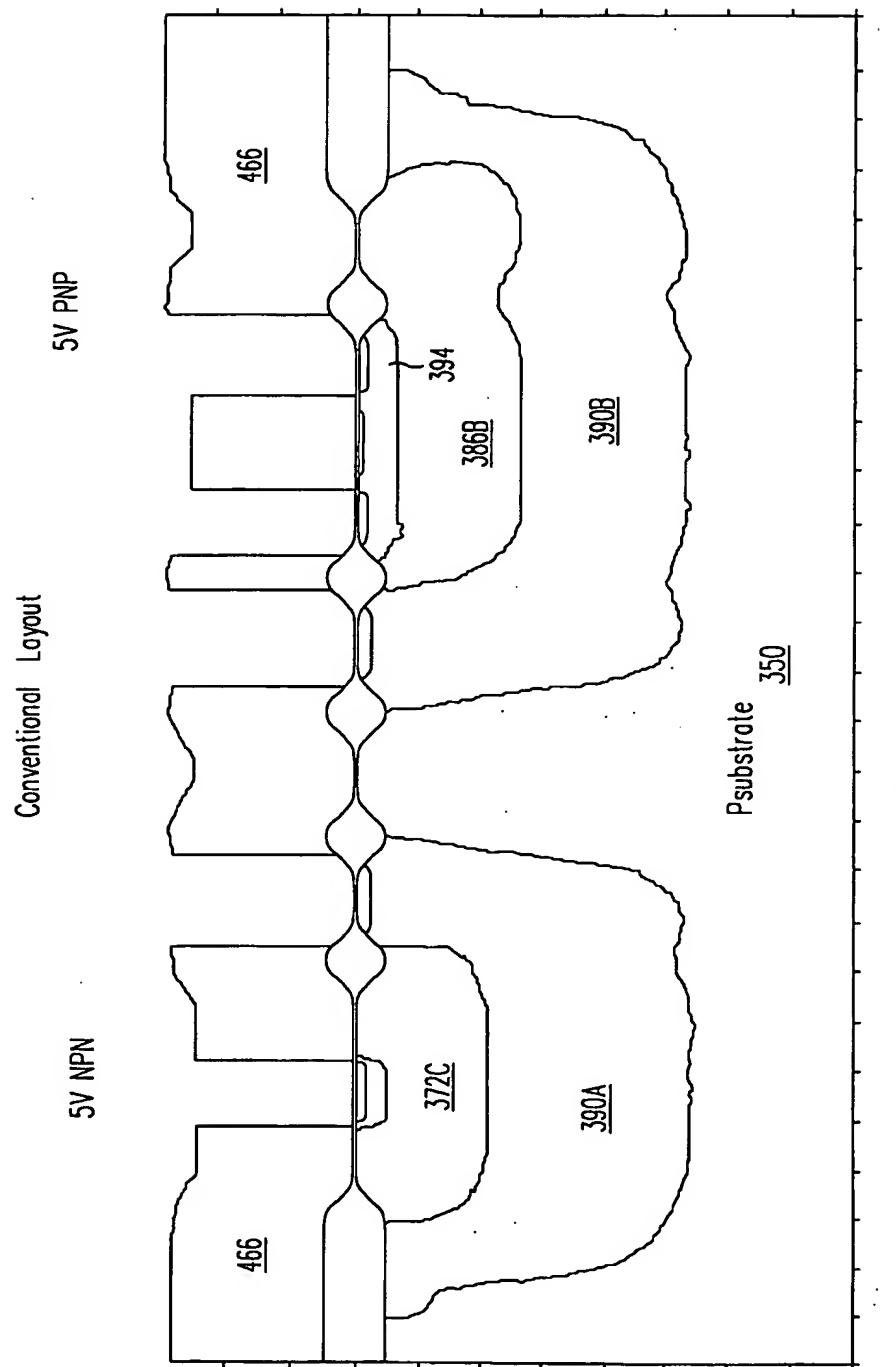
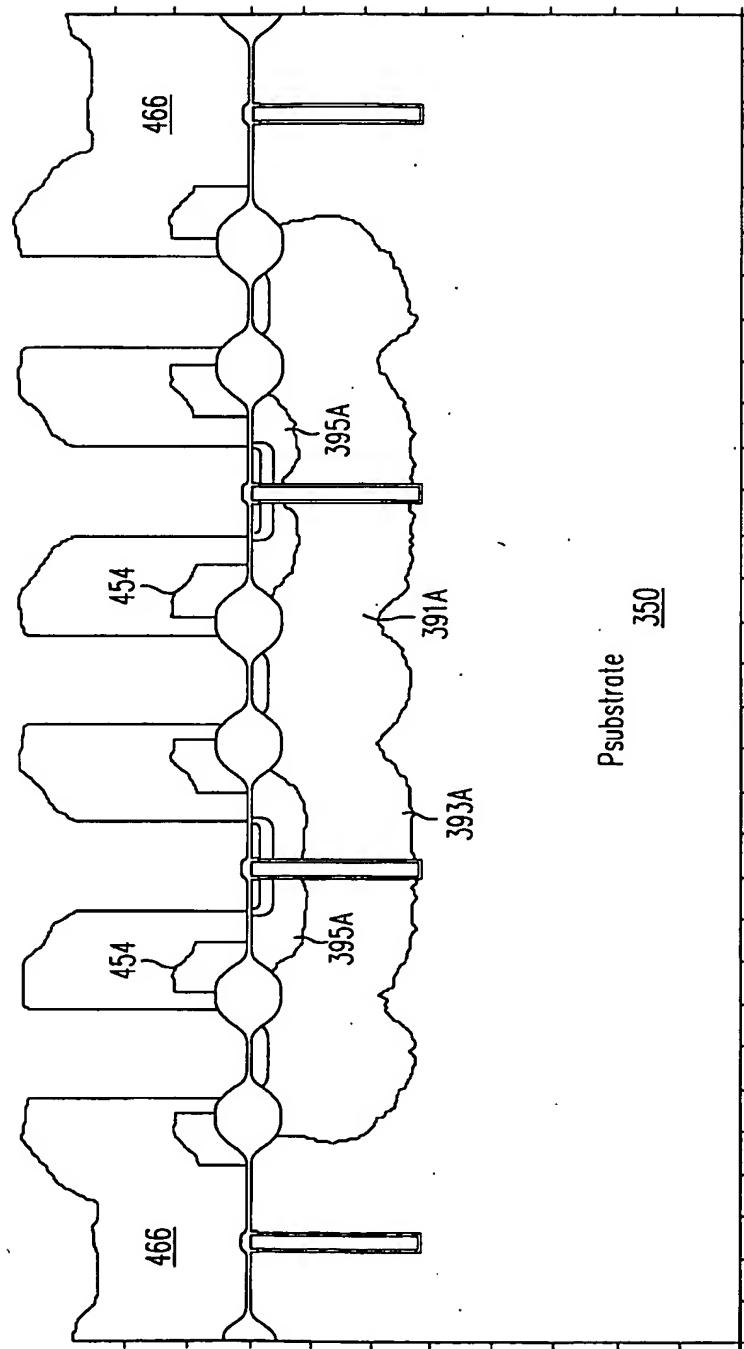


FIG. 60C

30V Lateral French DMOS — 308



5V N-LDD implant

FIG. 60D

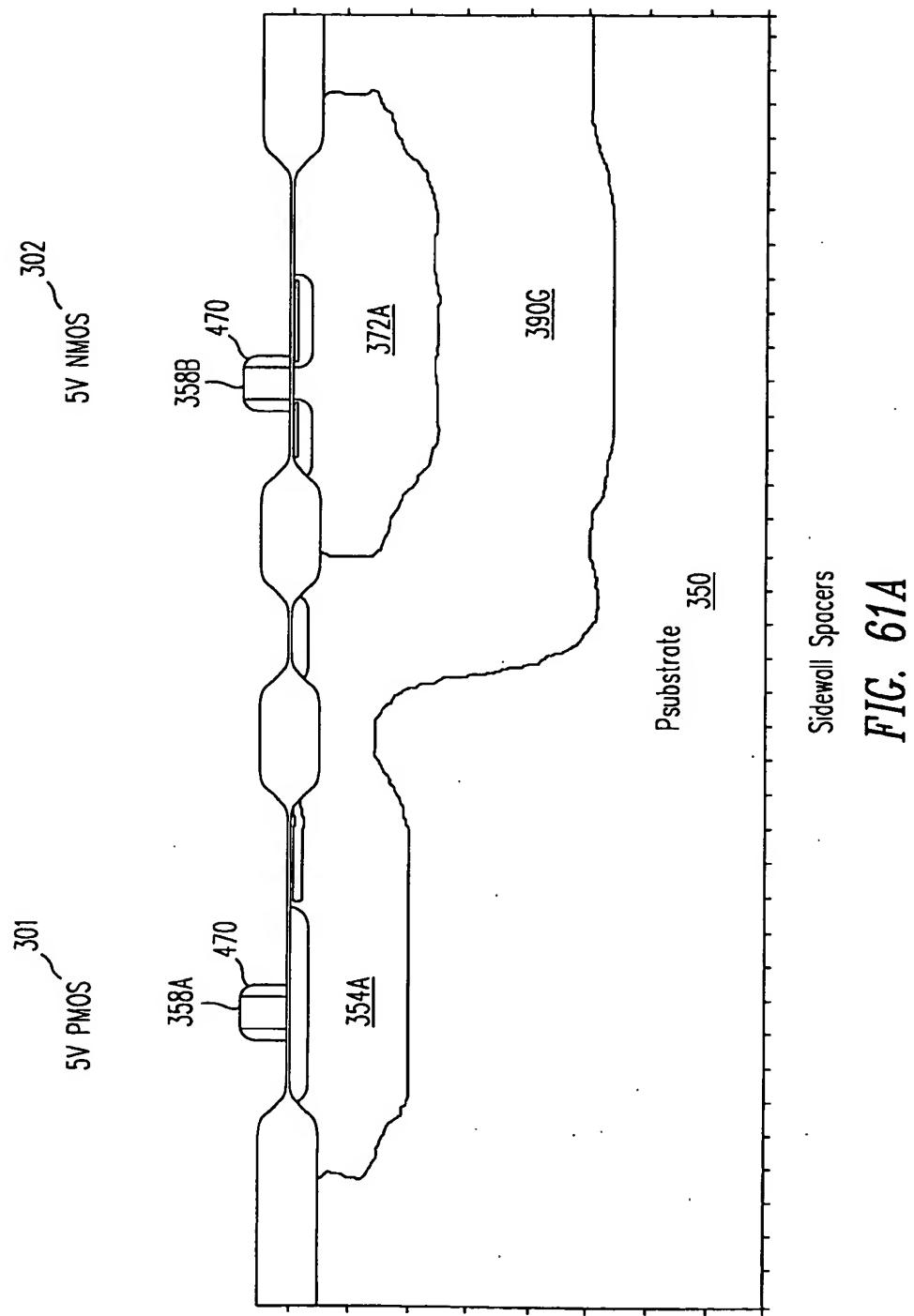
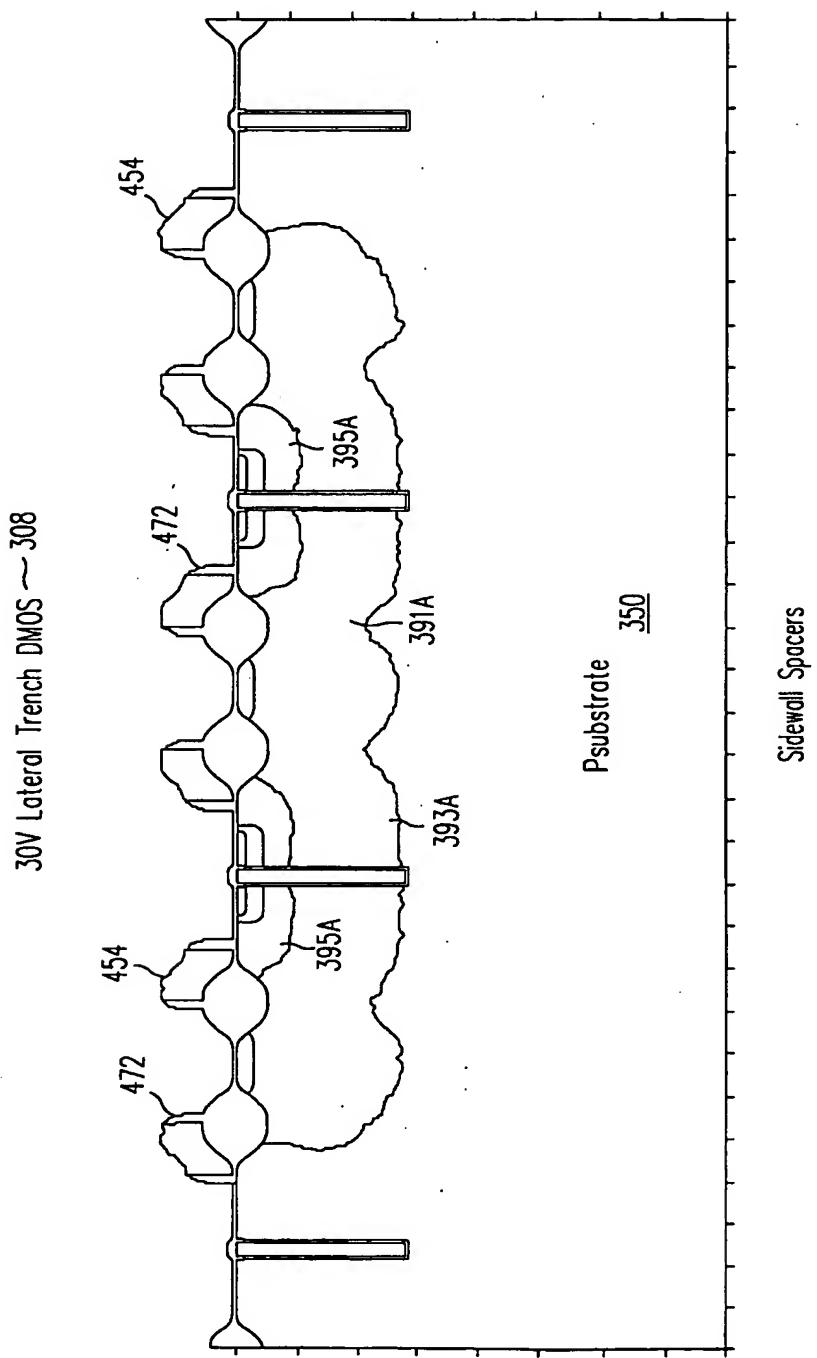
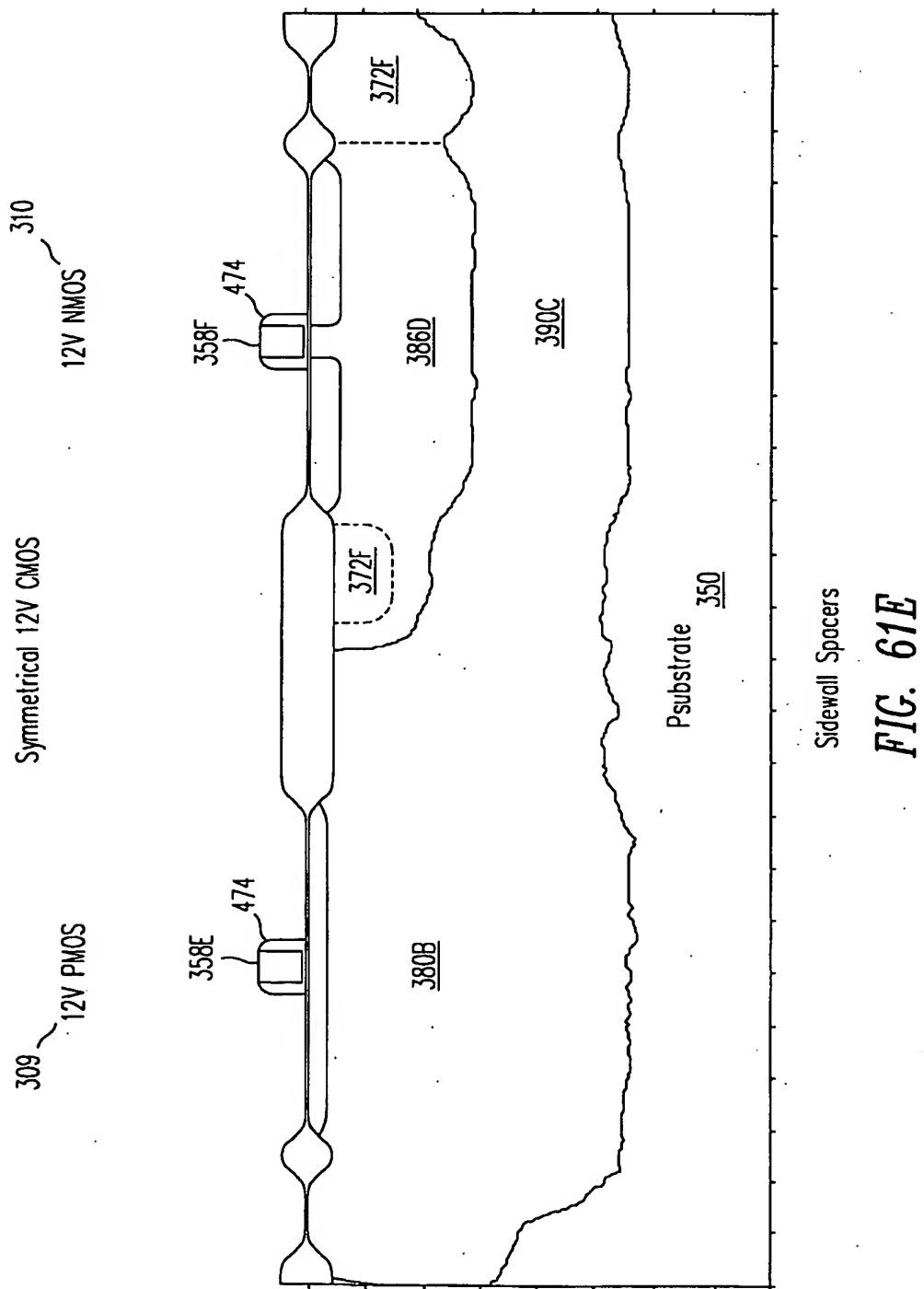
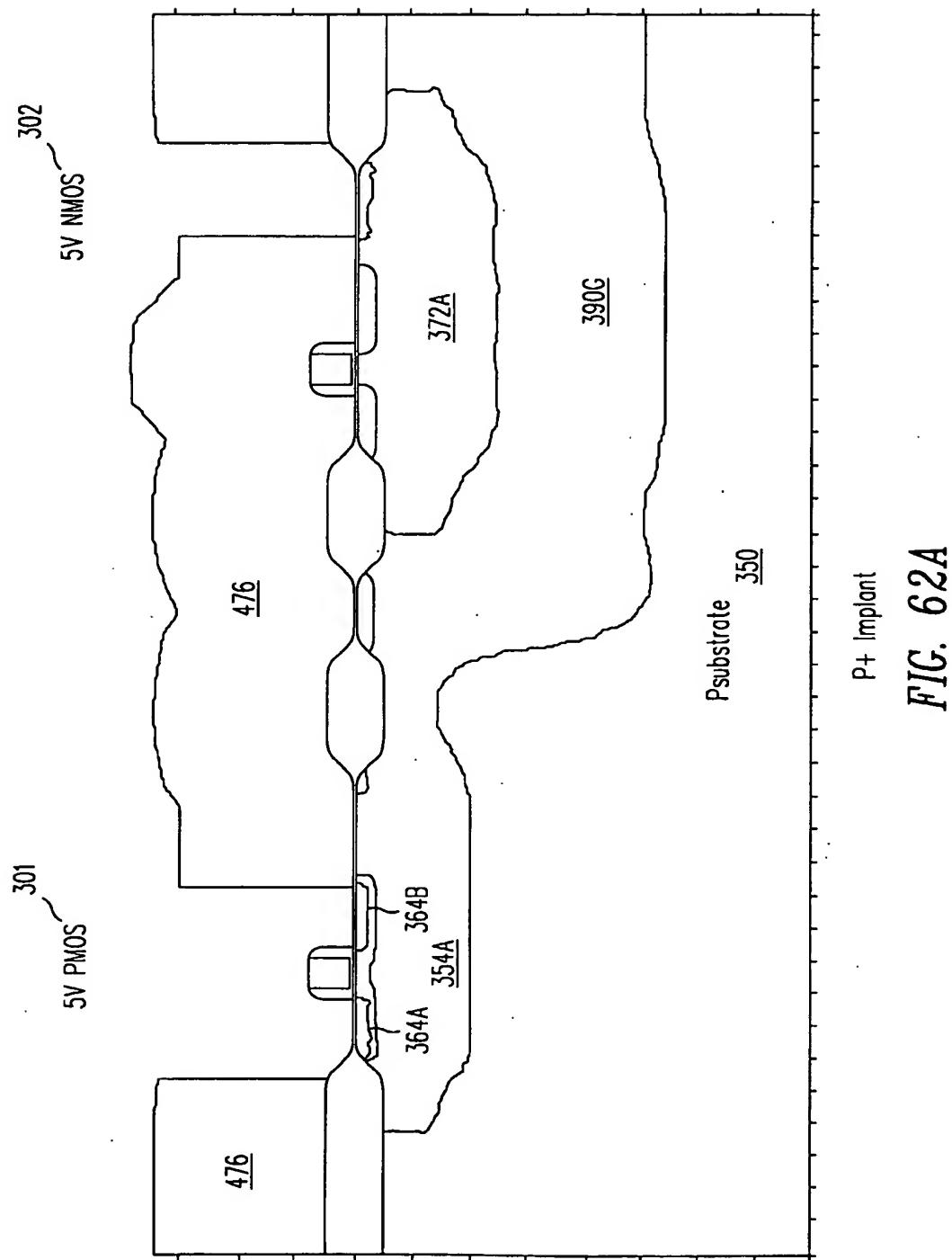


FIG. 61A



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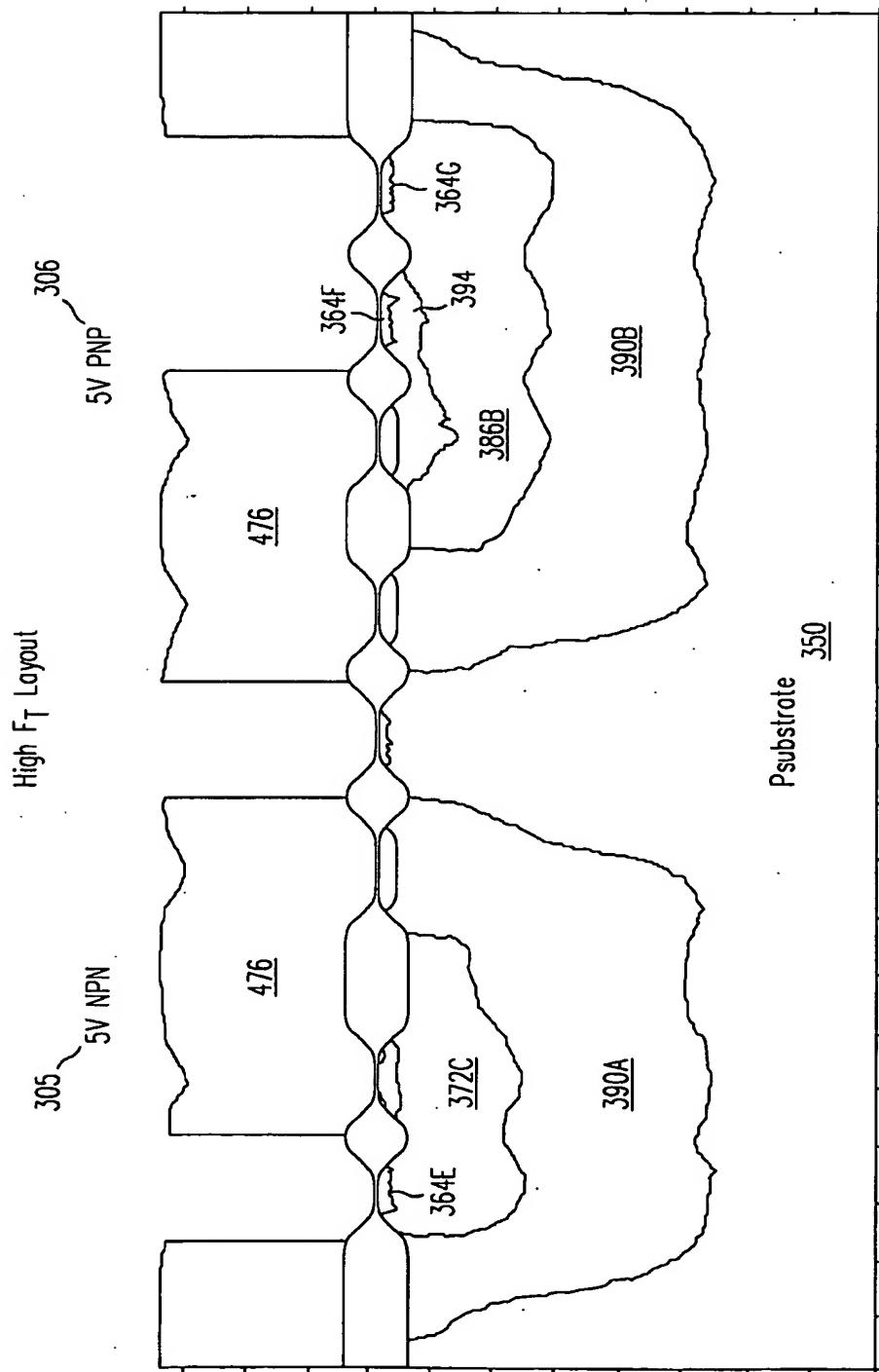
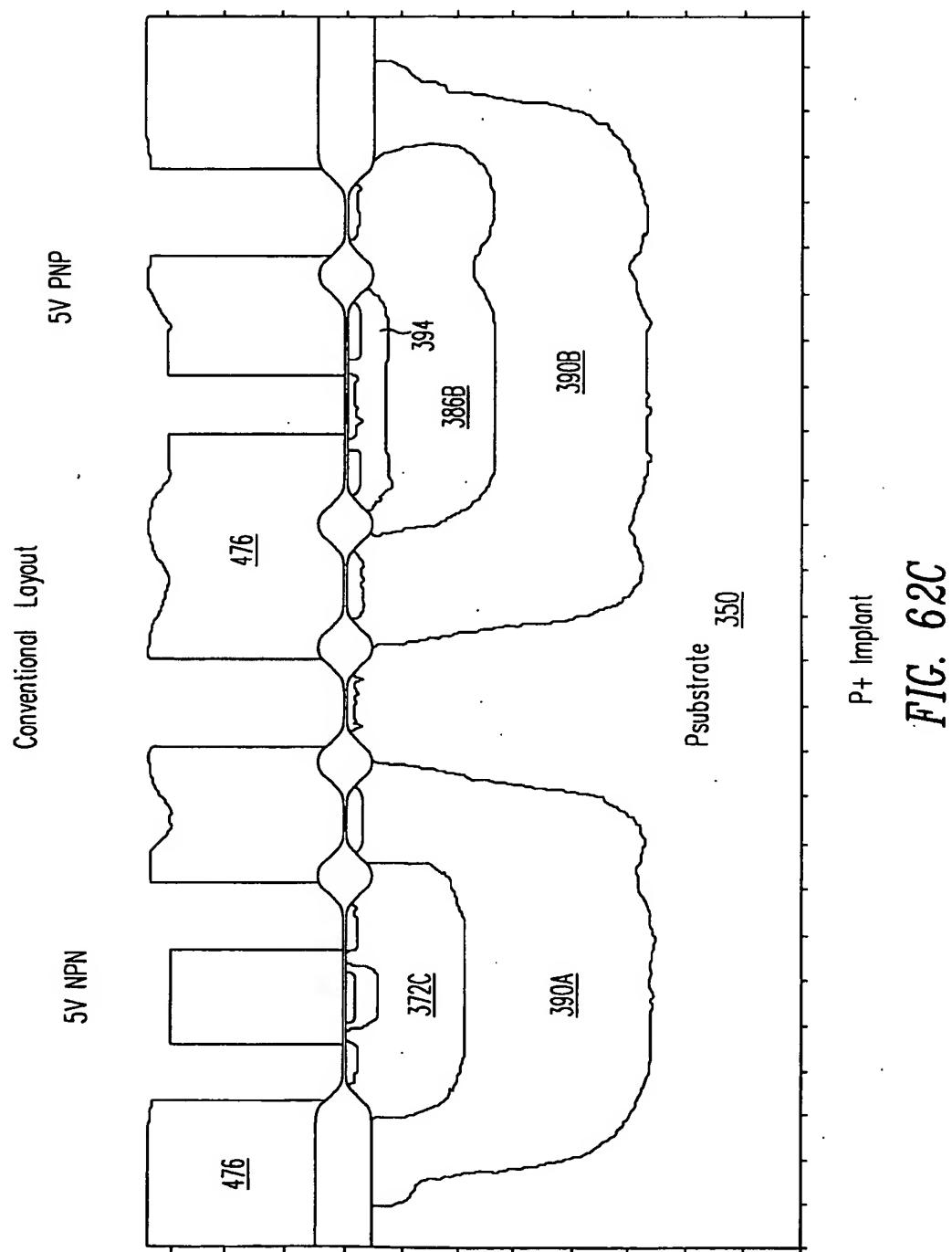


FIG. 62B



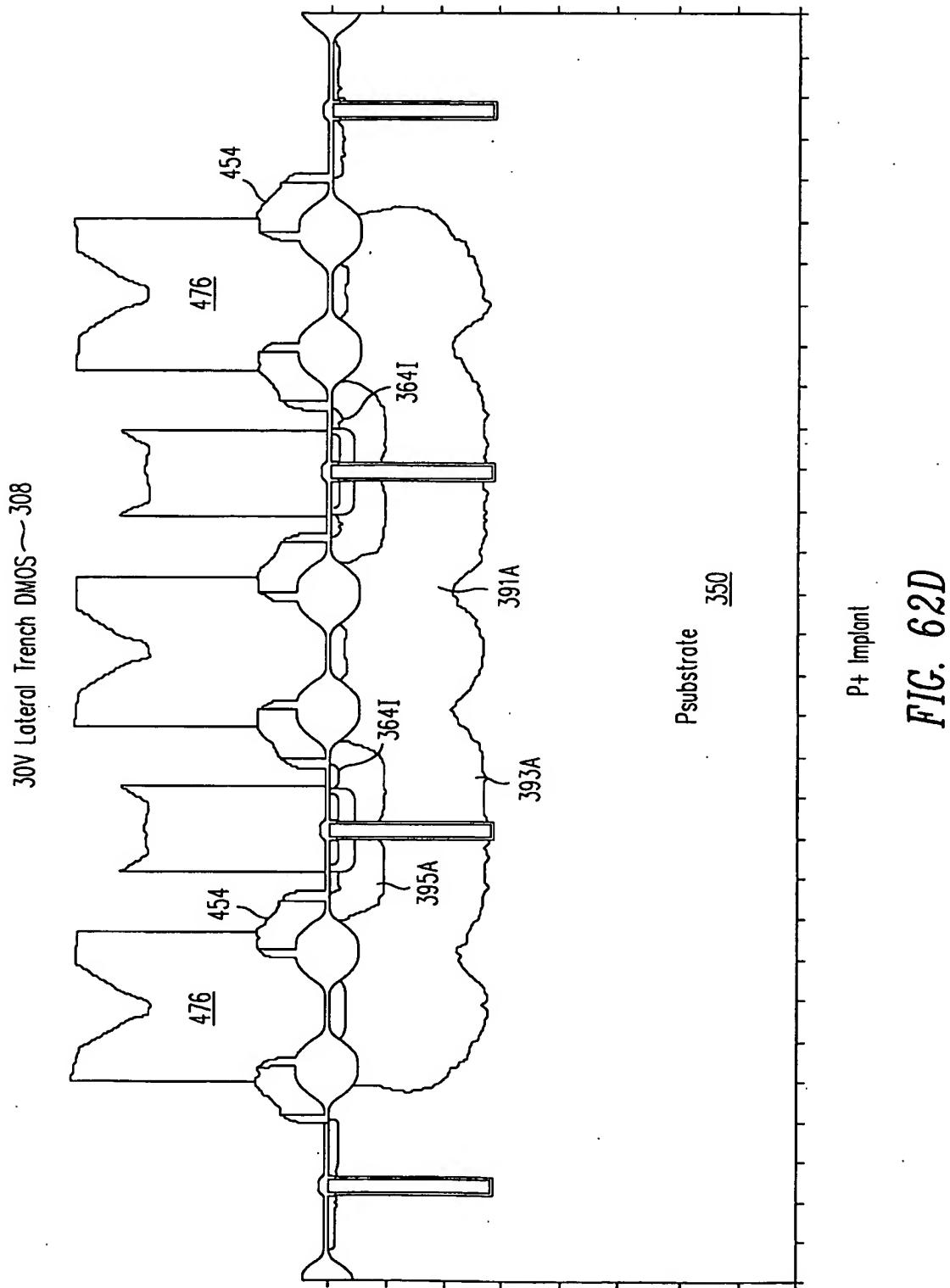
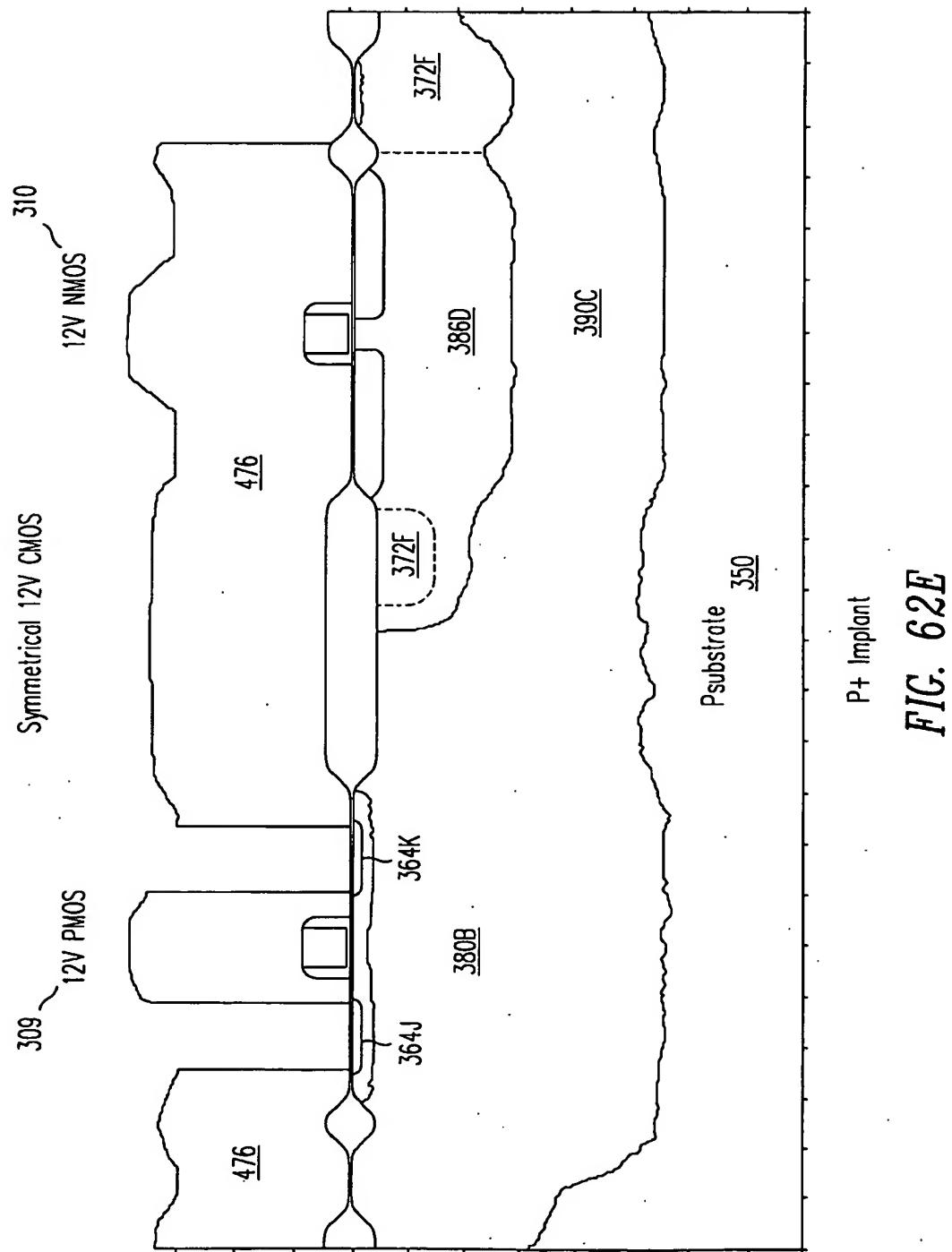


FIG. 62D

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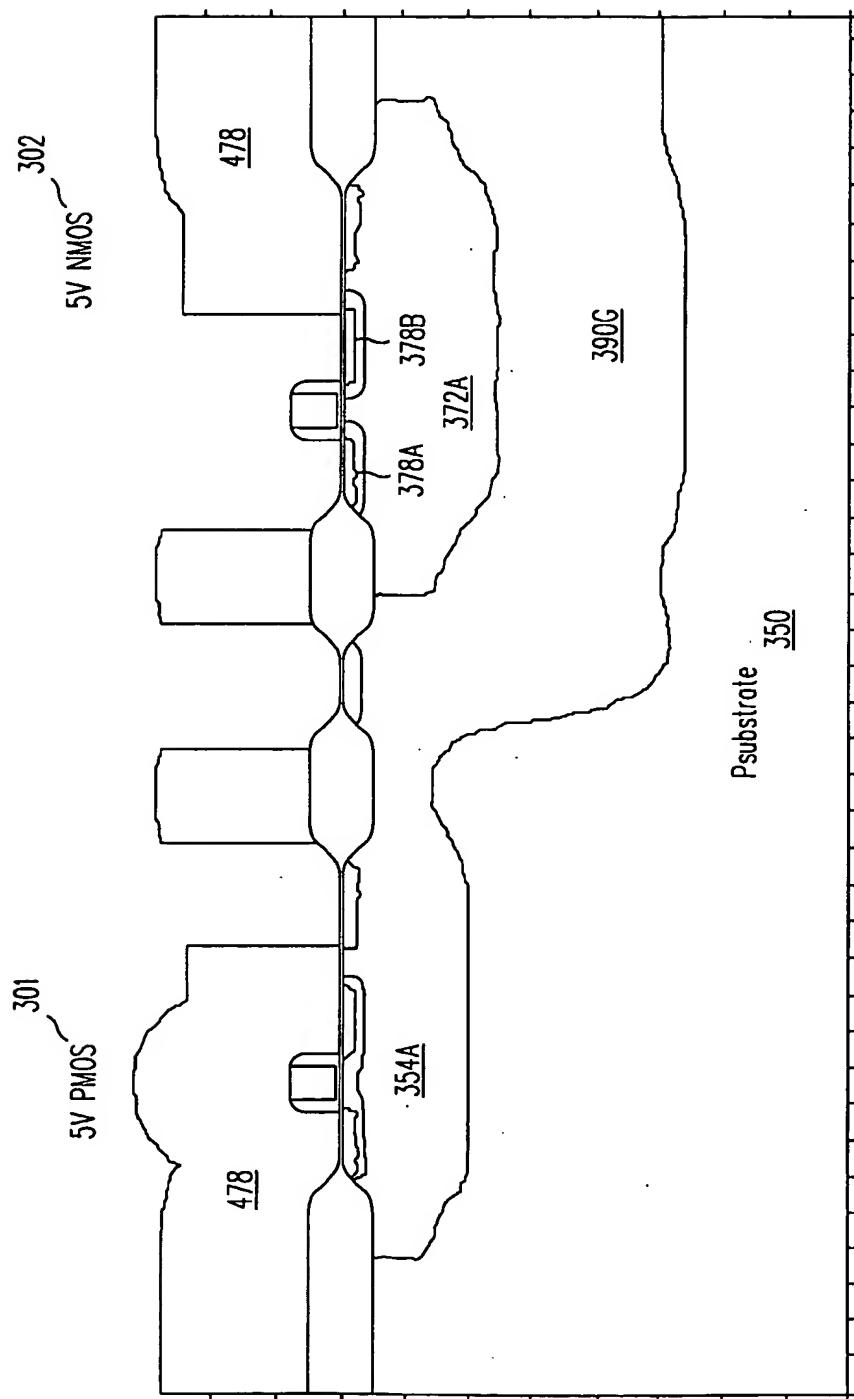
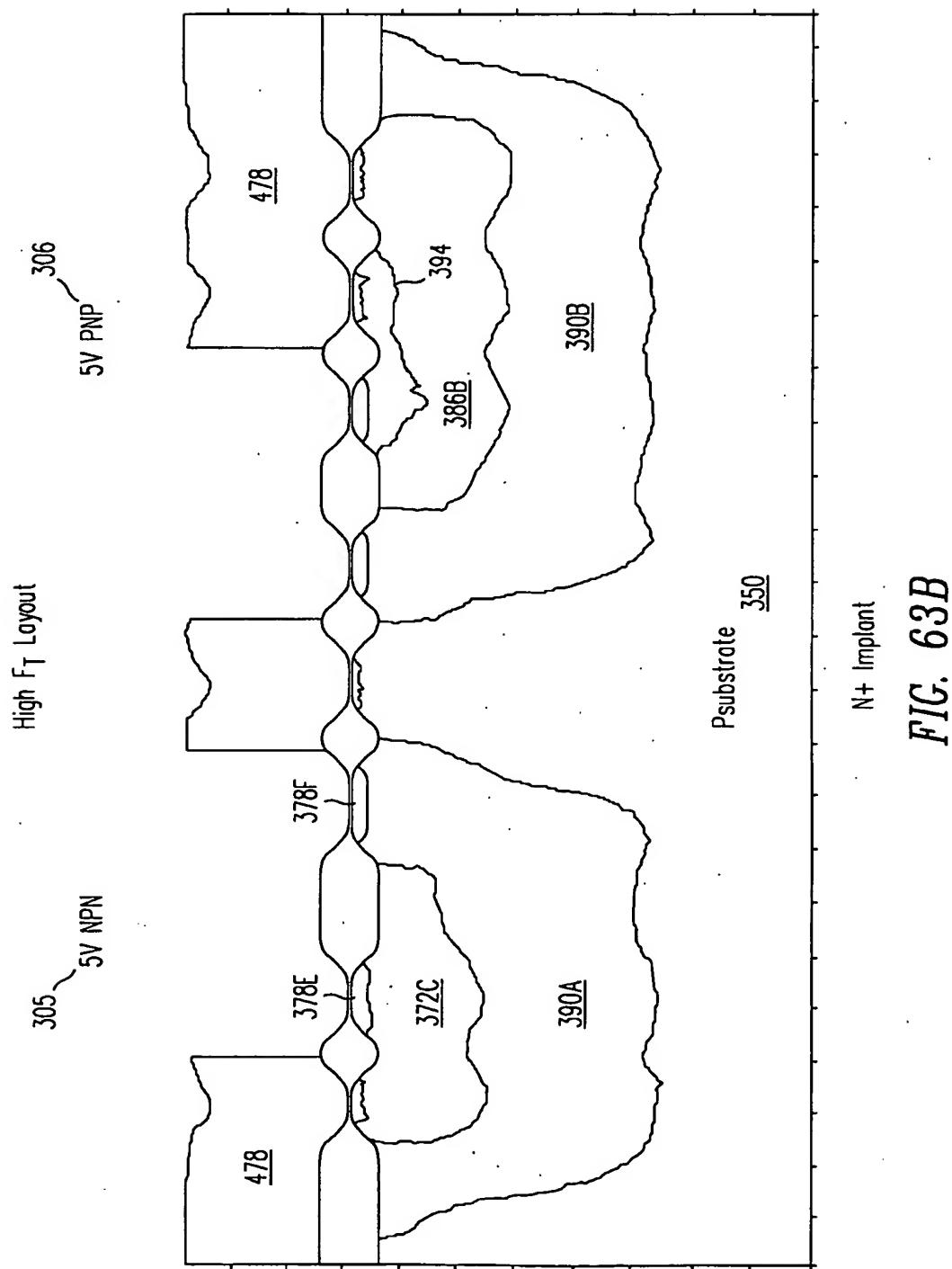


FIG. 634

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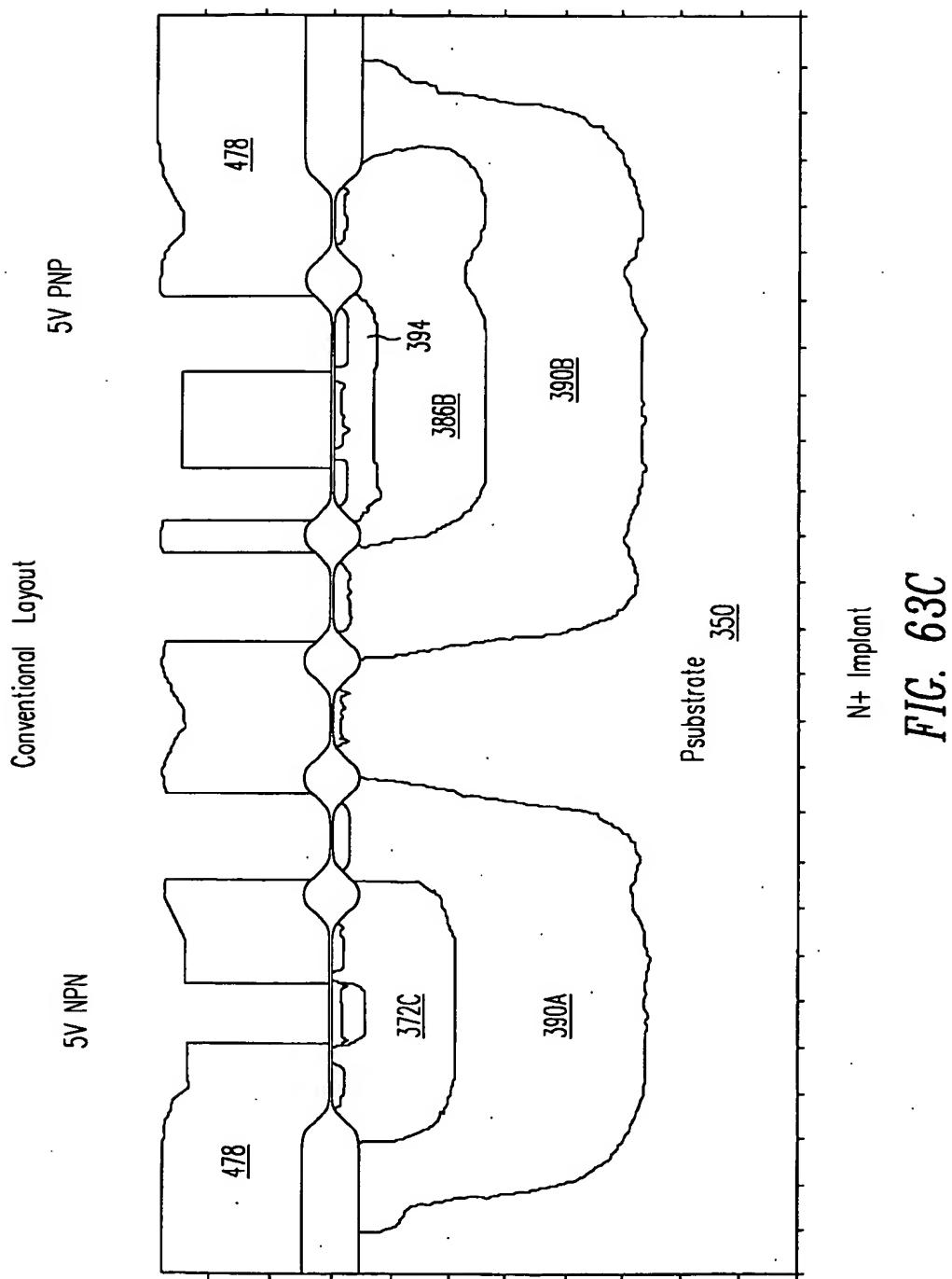
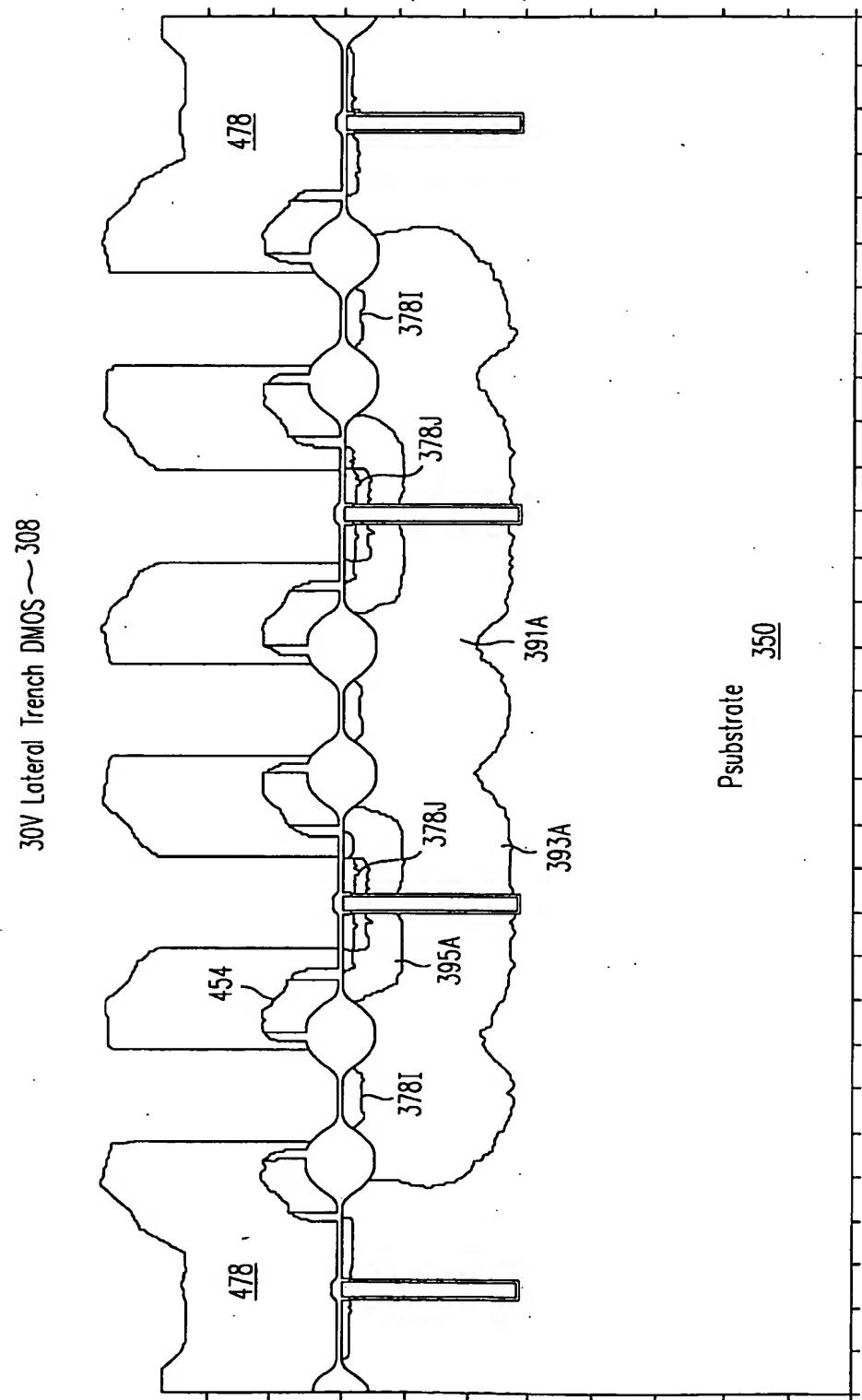


FIG. 63C

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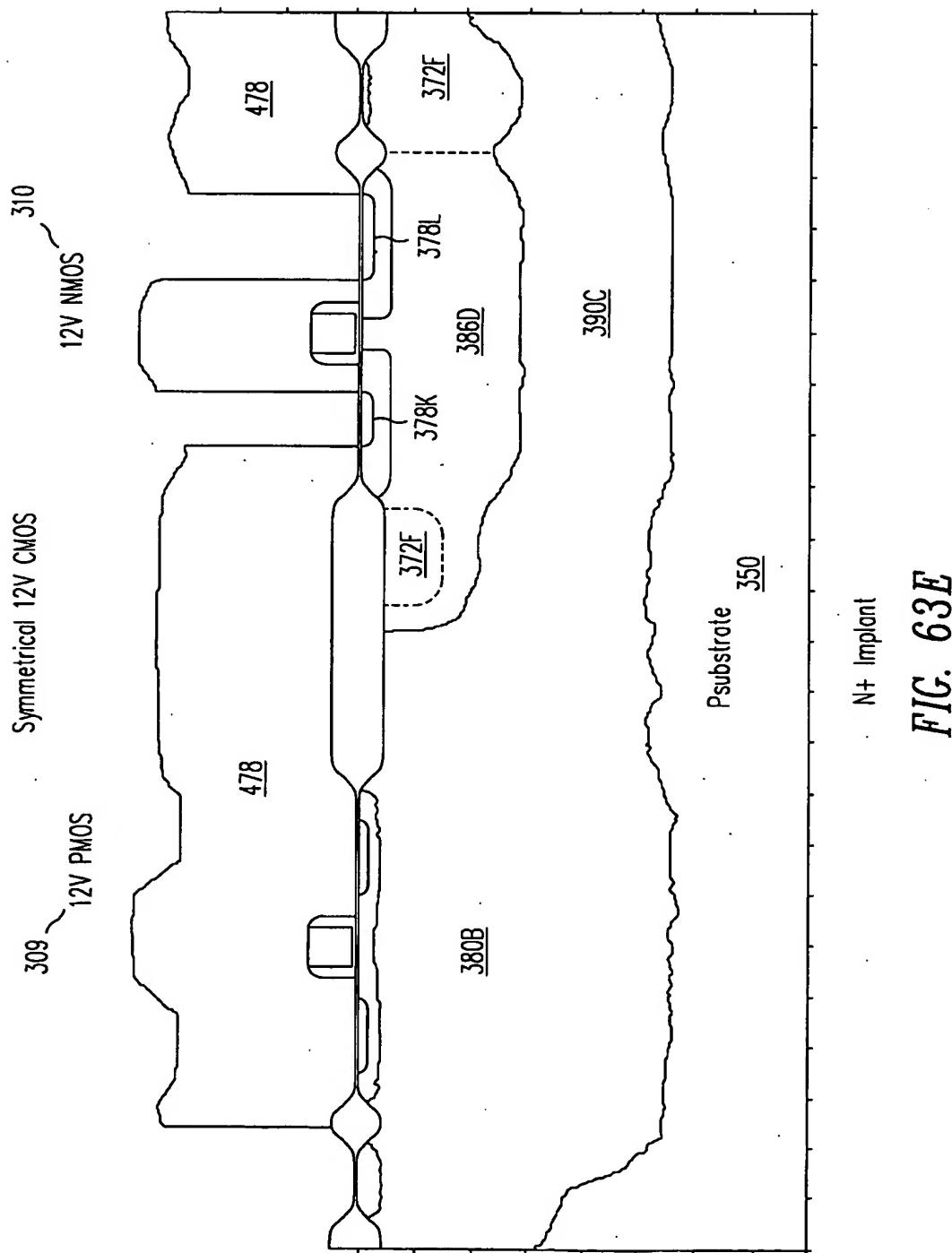
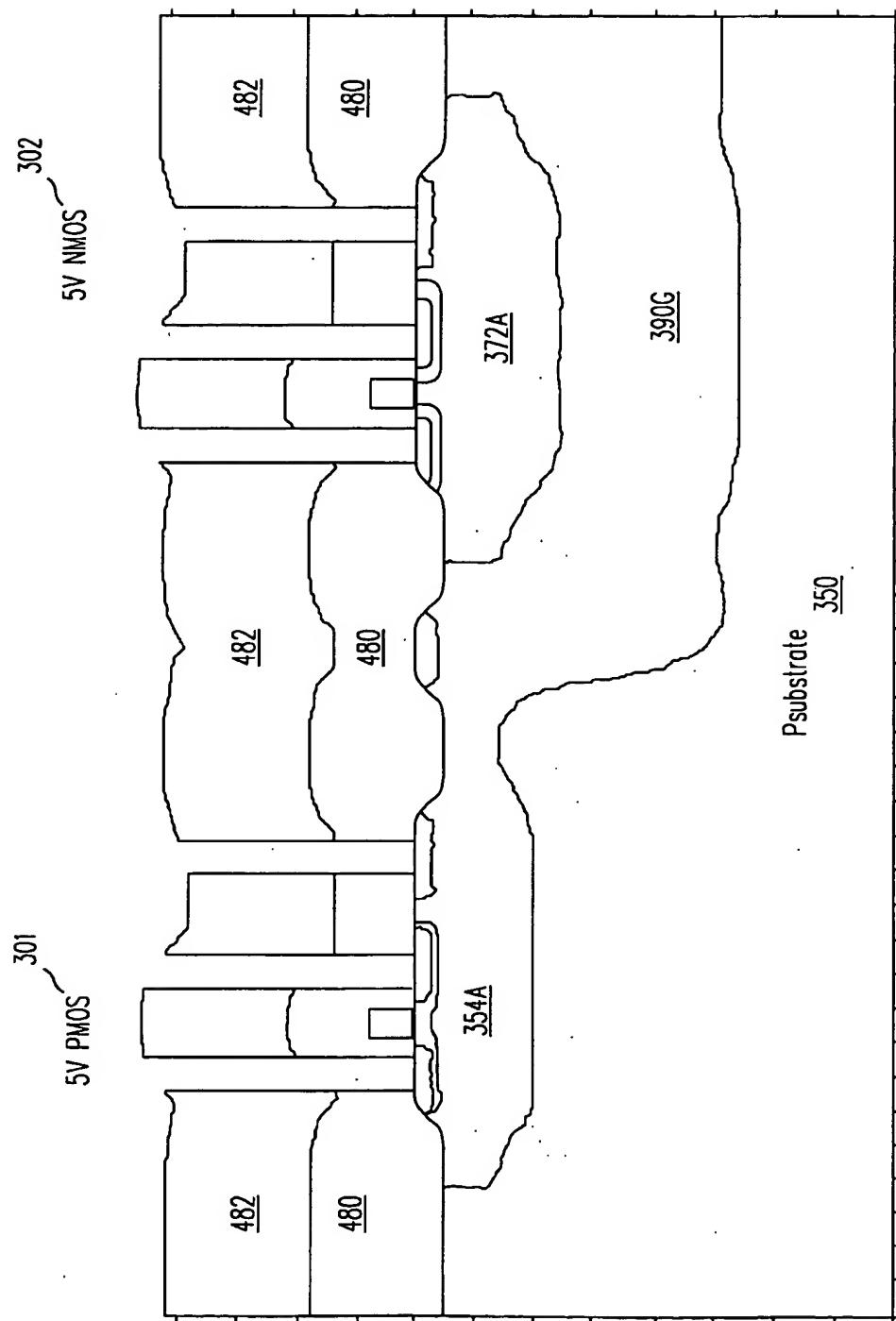
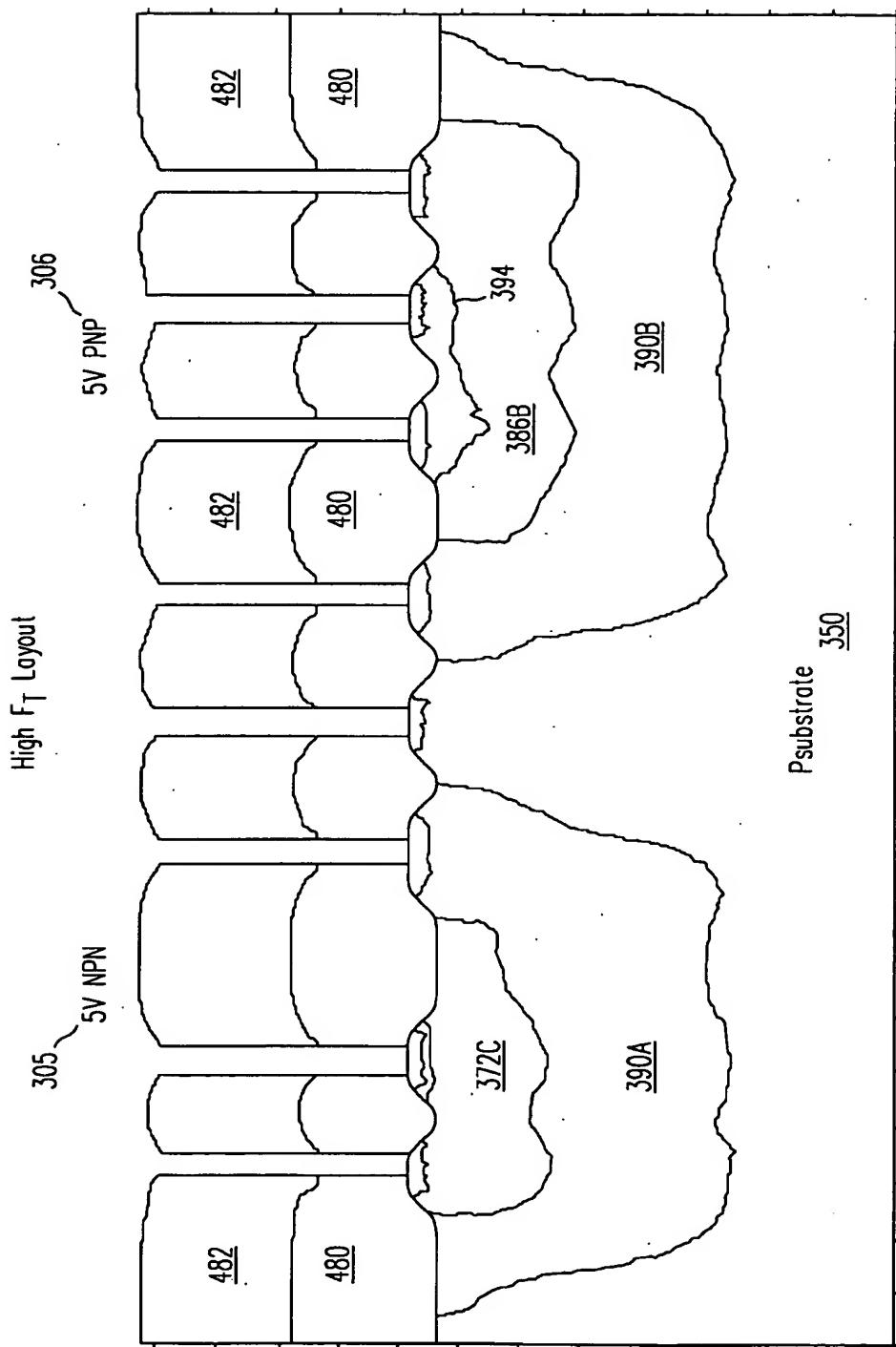


FIG. 63E



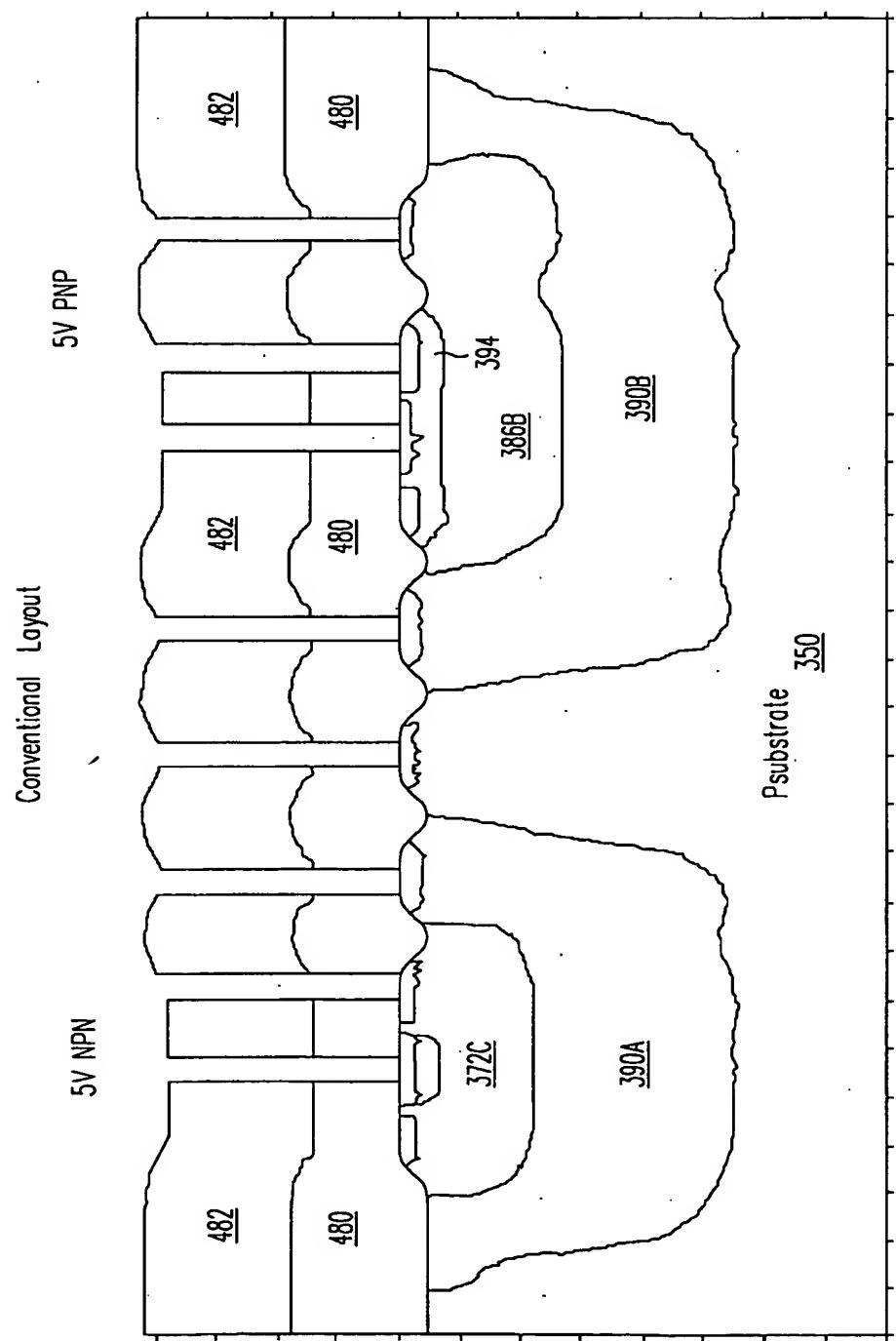
Interlayer Dielectric Deposition and Etch

FIG. 64A



Interlayer Dielectric Deposition and Etch

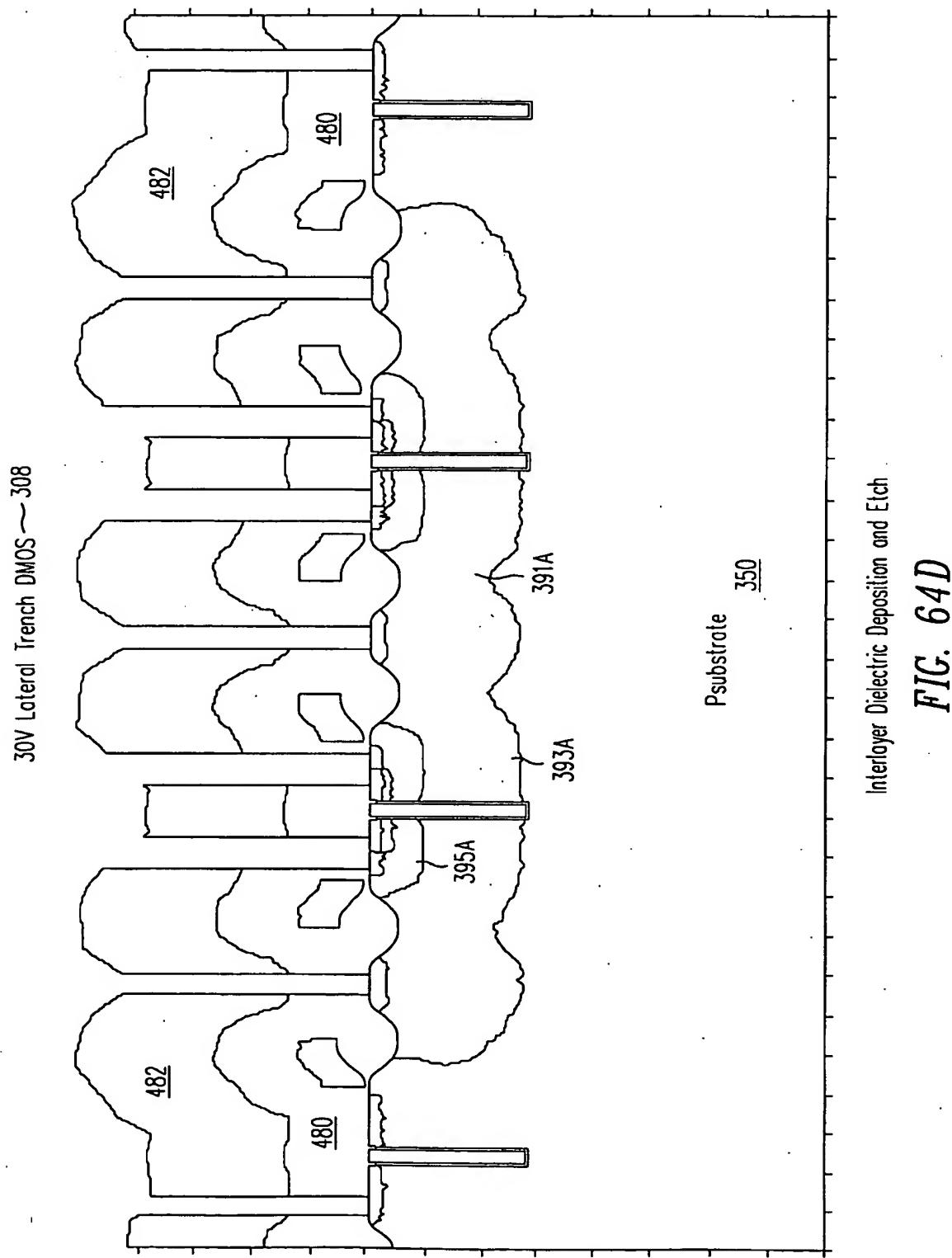
FIG. 64B

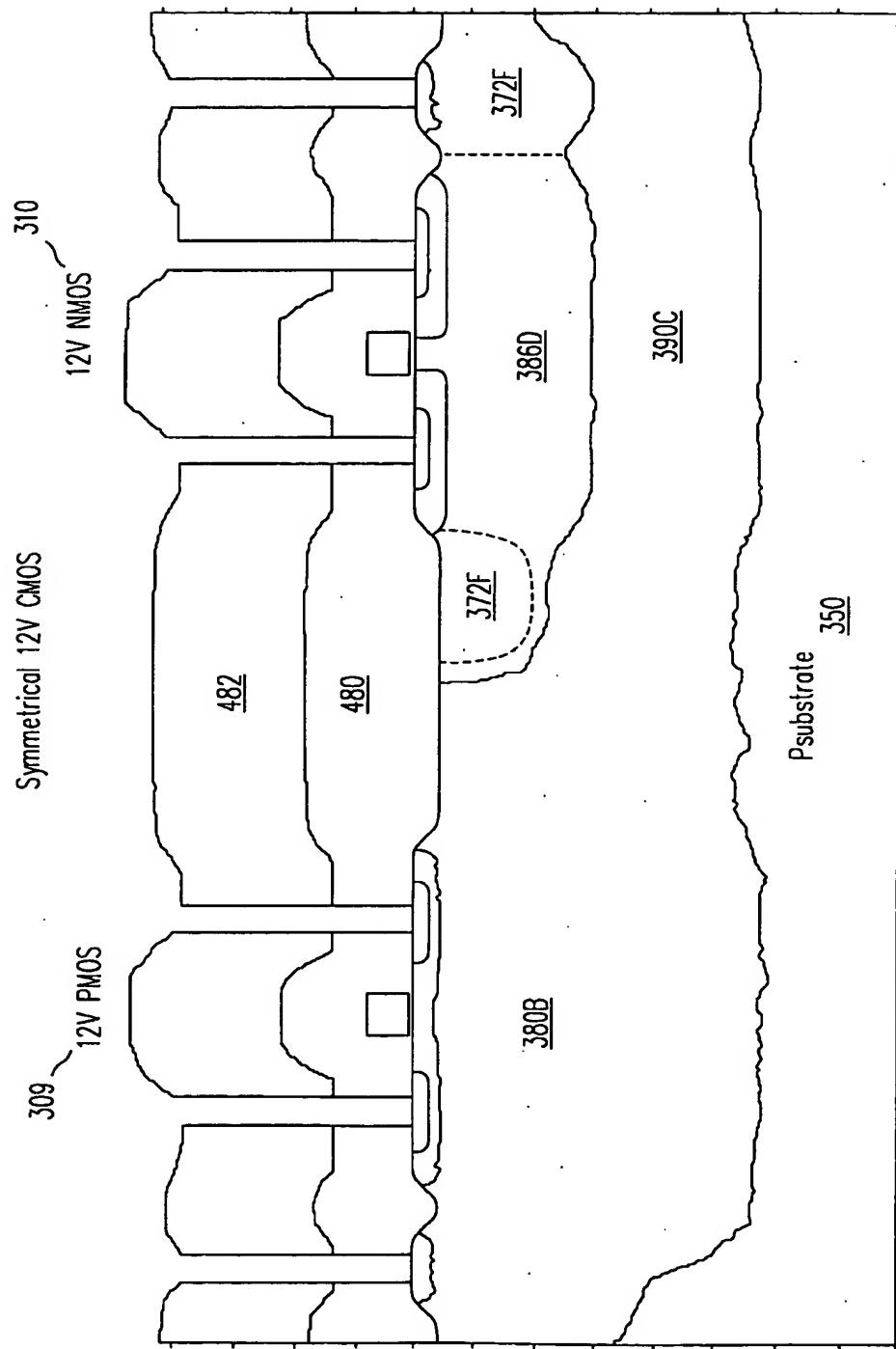


Interlayer Dielectric Deposition and Etch

FIG. 64C

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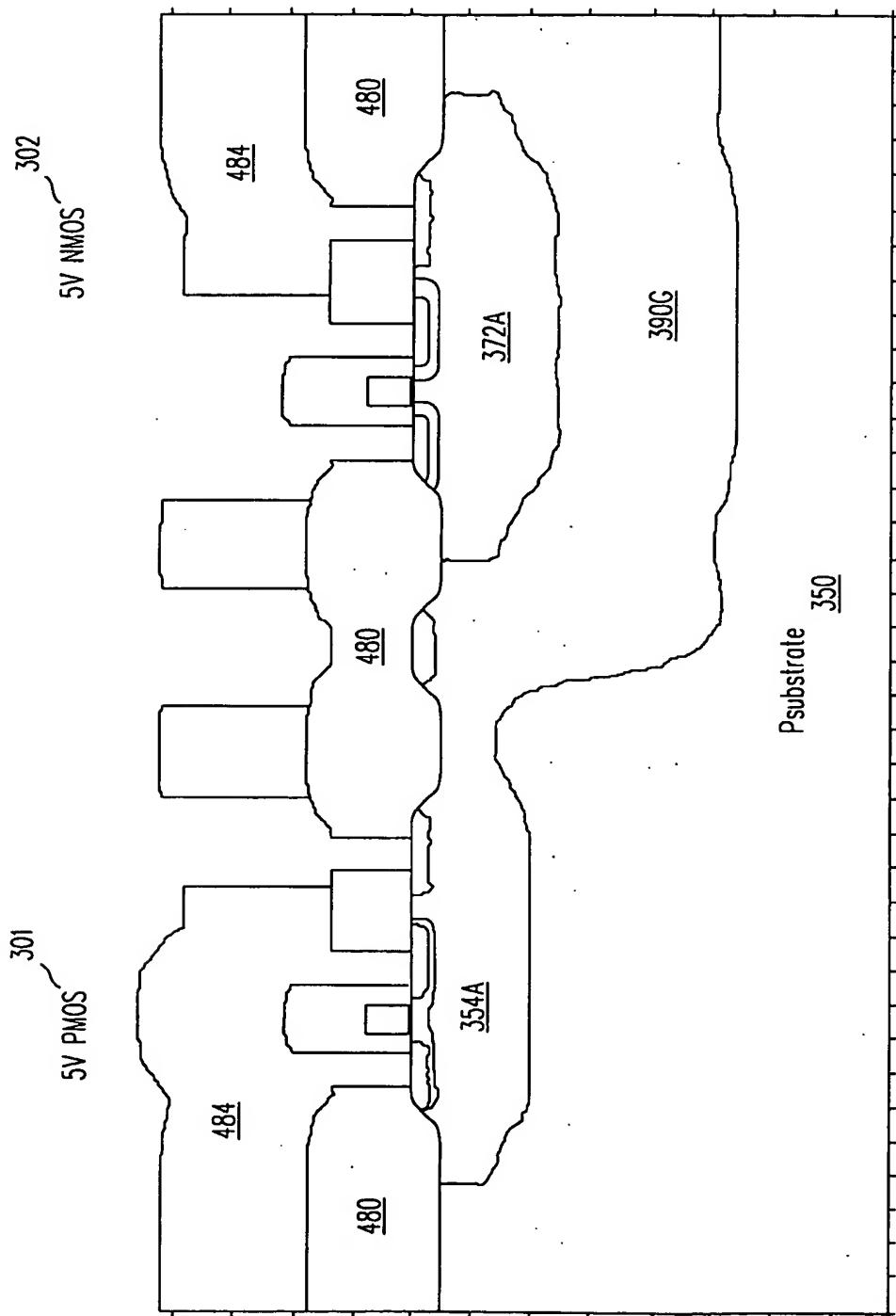




Interlayer Dielectric Deposition and Etch

FIG. 64E

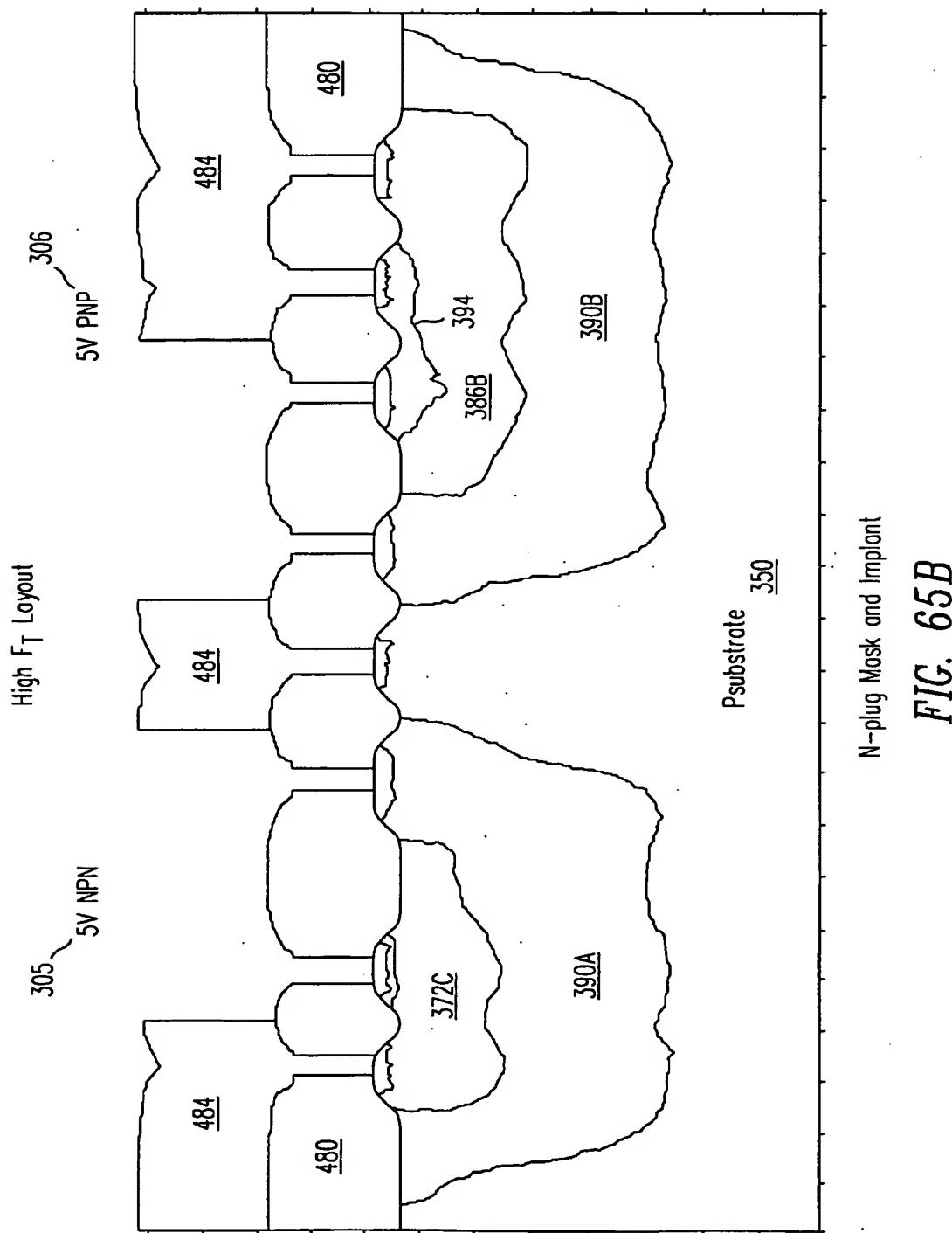
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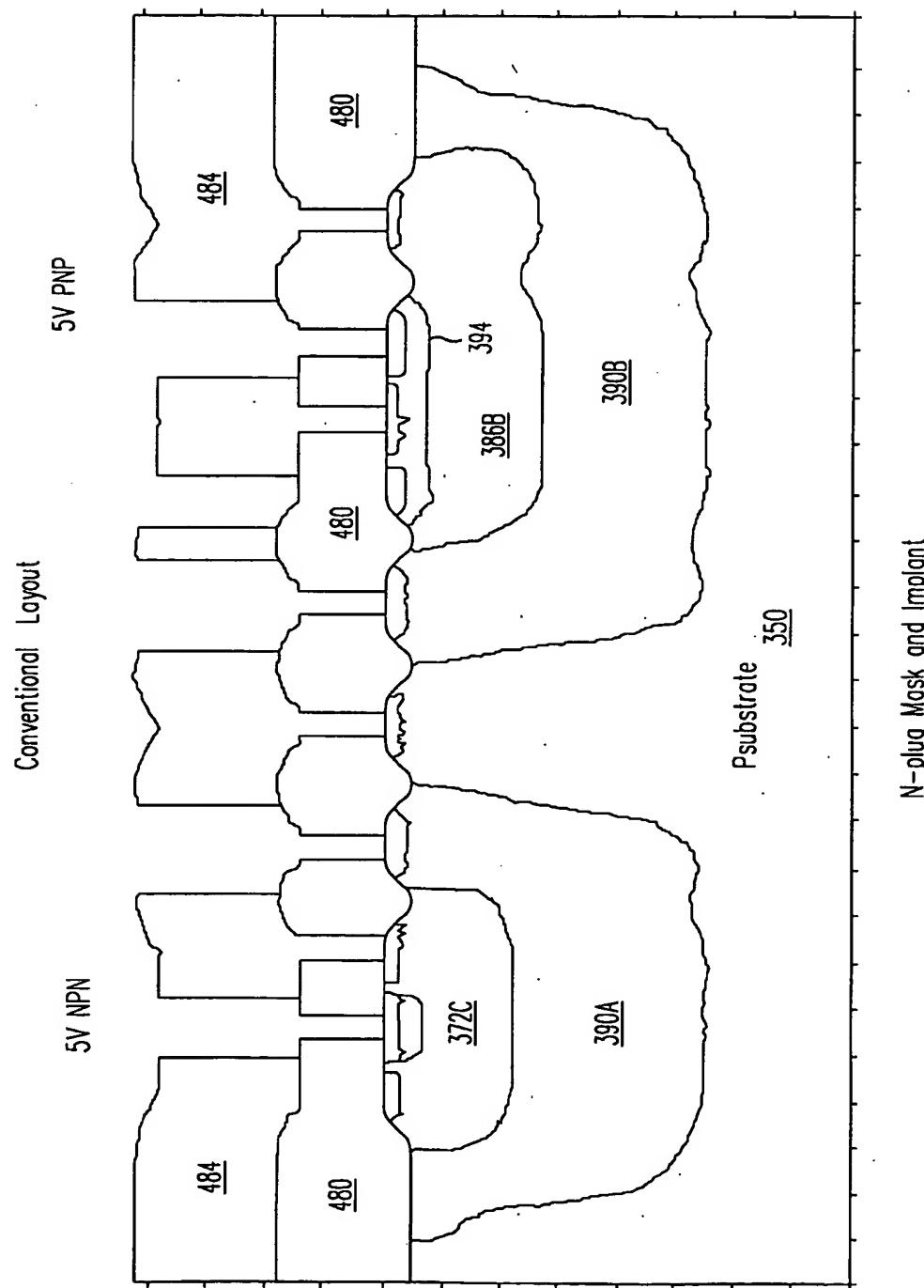


N-plug Mask and Implant

FIG. 65A

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N-plug Mask and Implant
FIG. 65C

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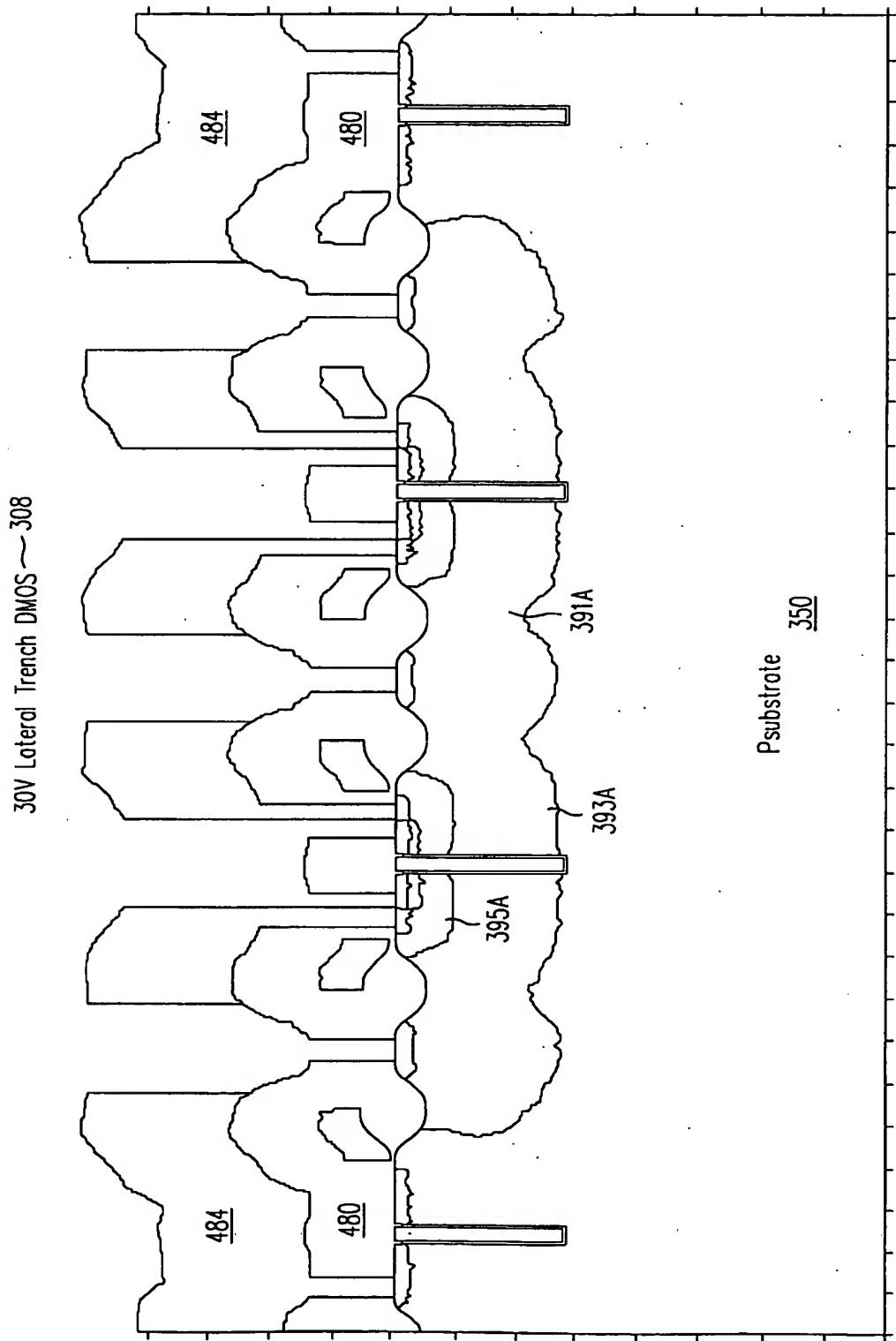
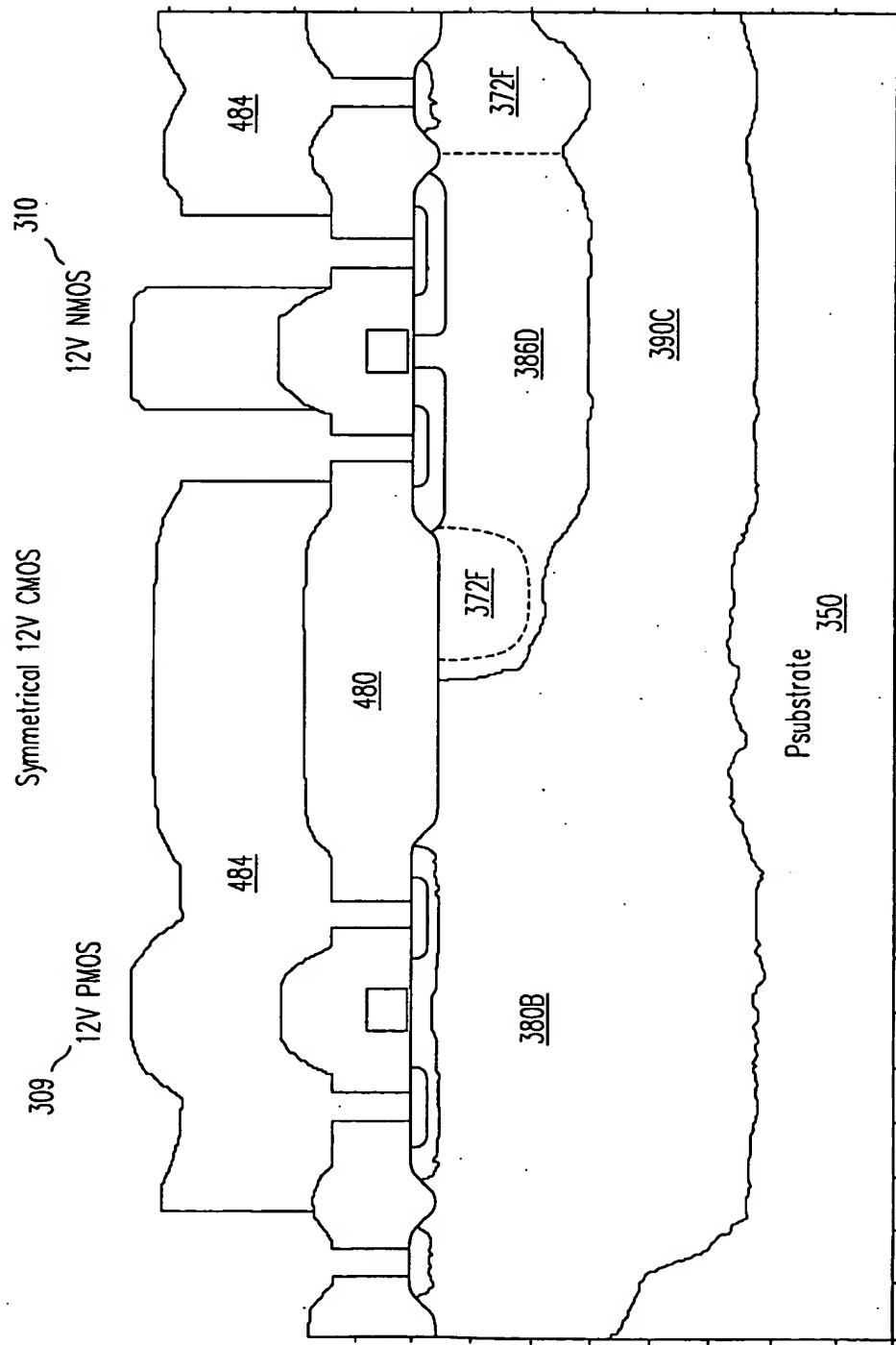


FIG. 65D

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N-plug Mask and implant

FIG. 65E

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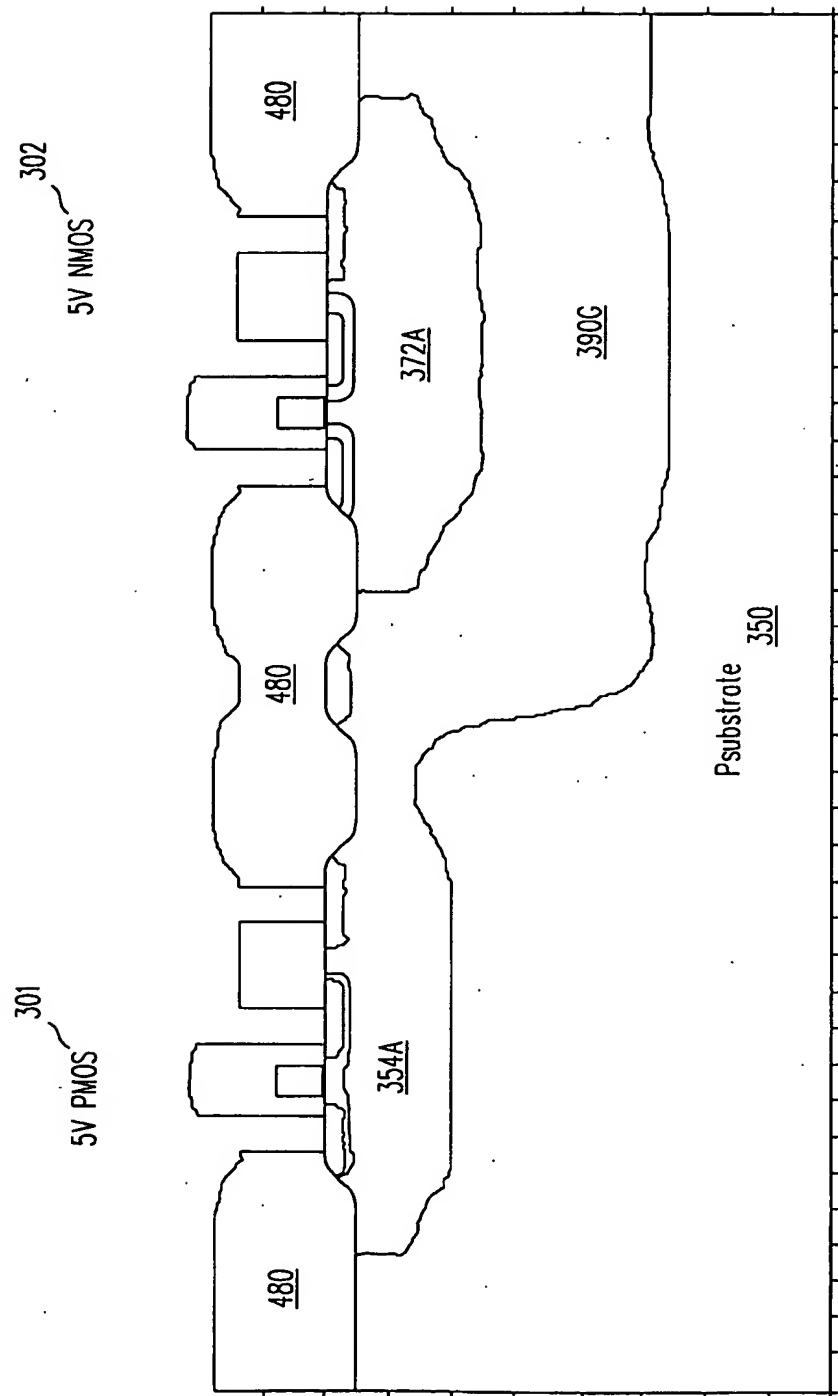
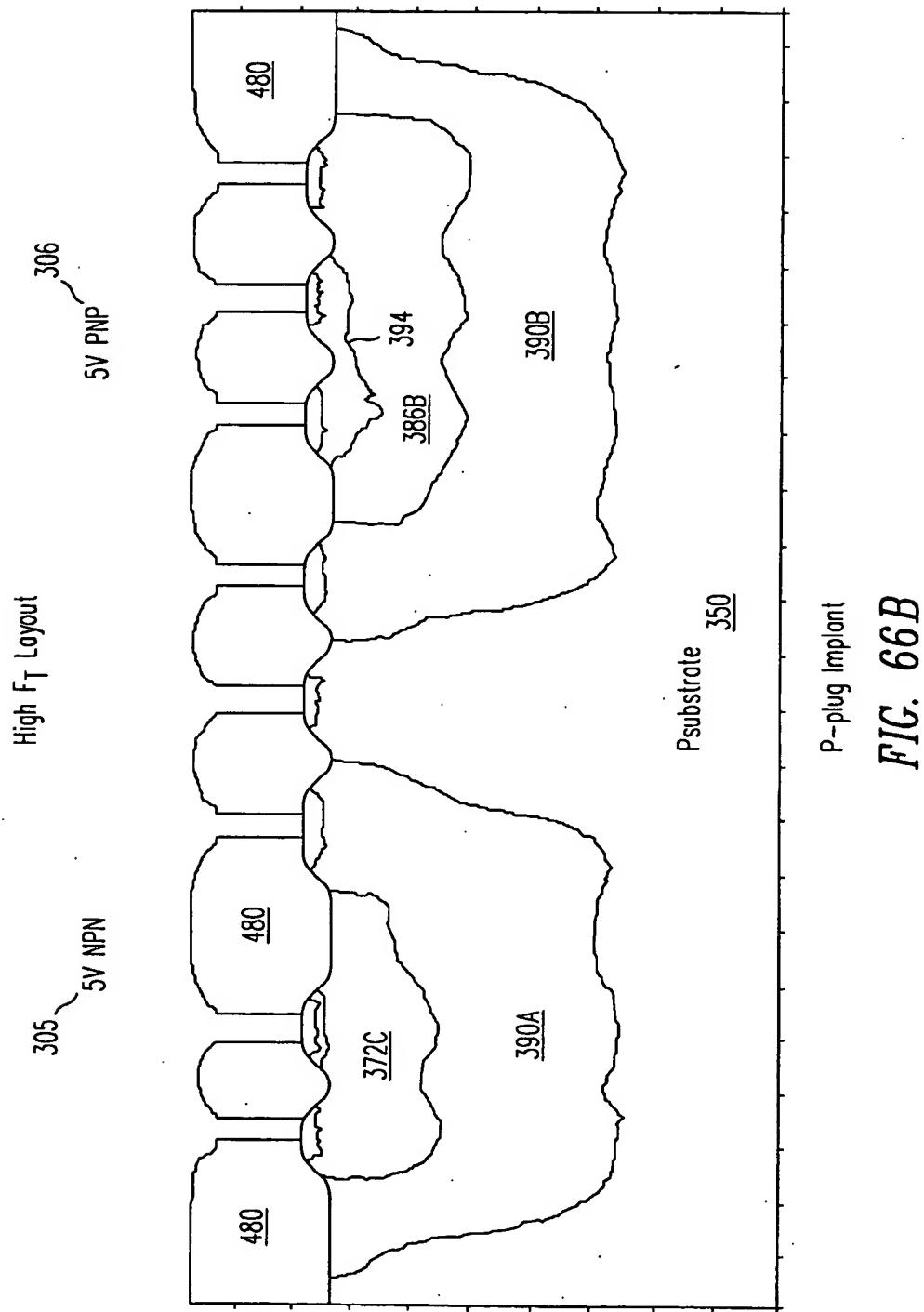


FIG. 66A

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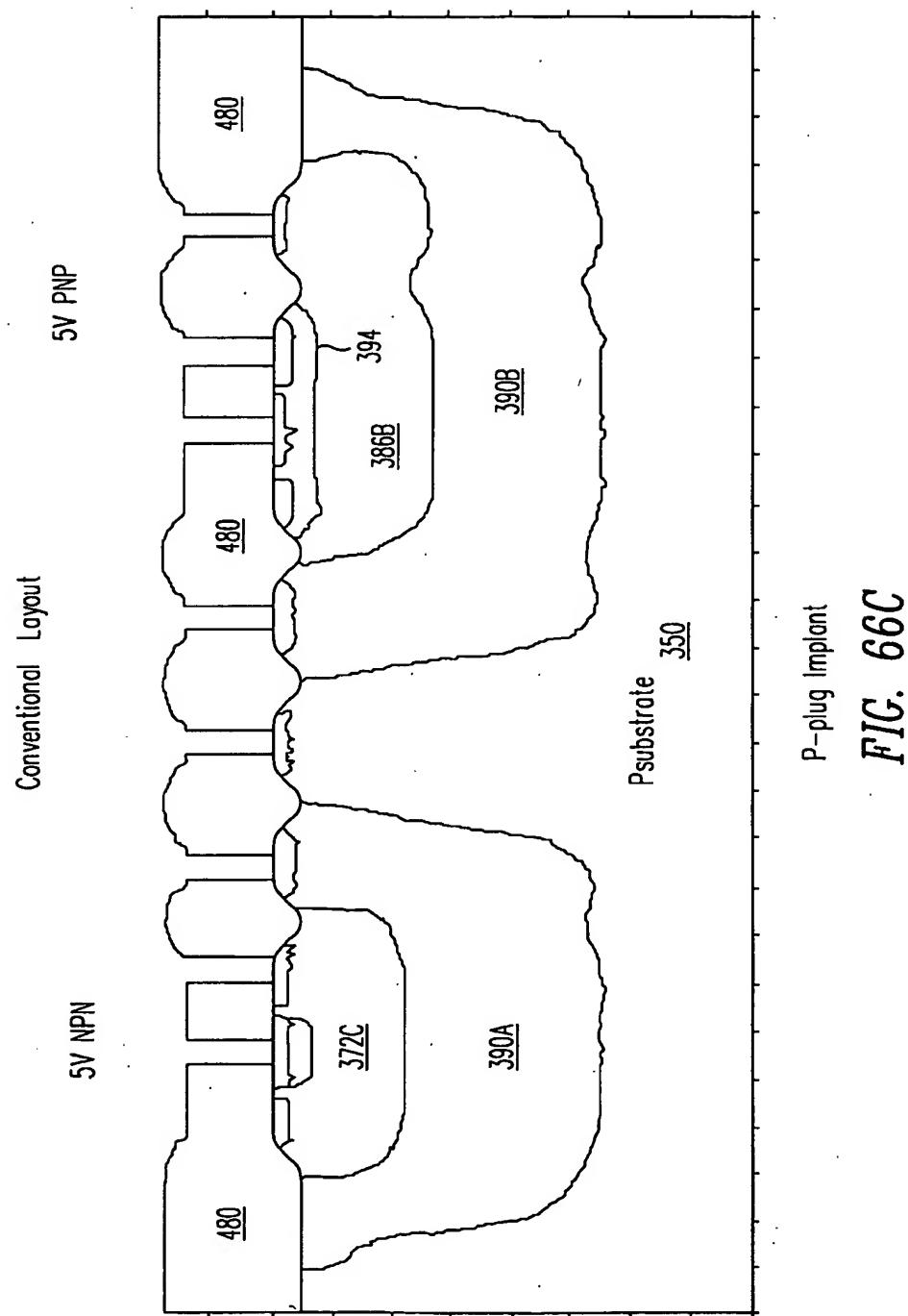
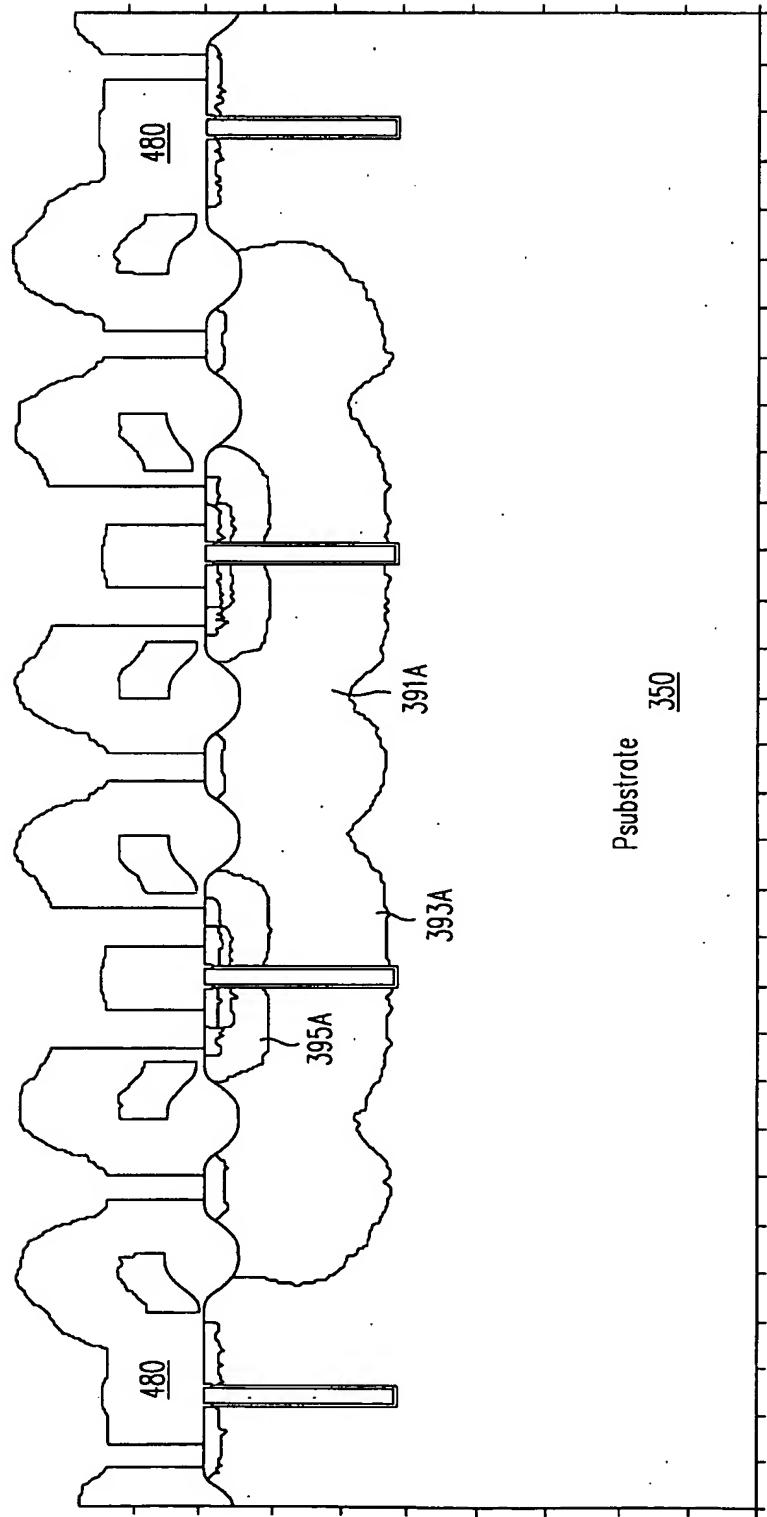


FIG. 66C

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30V Lateral Trench DMOS ~ 308



P-plug implant
FIG. 66D

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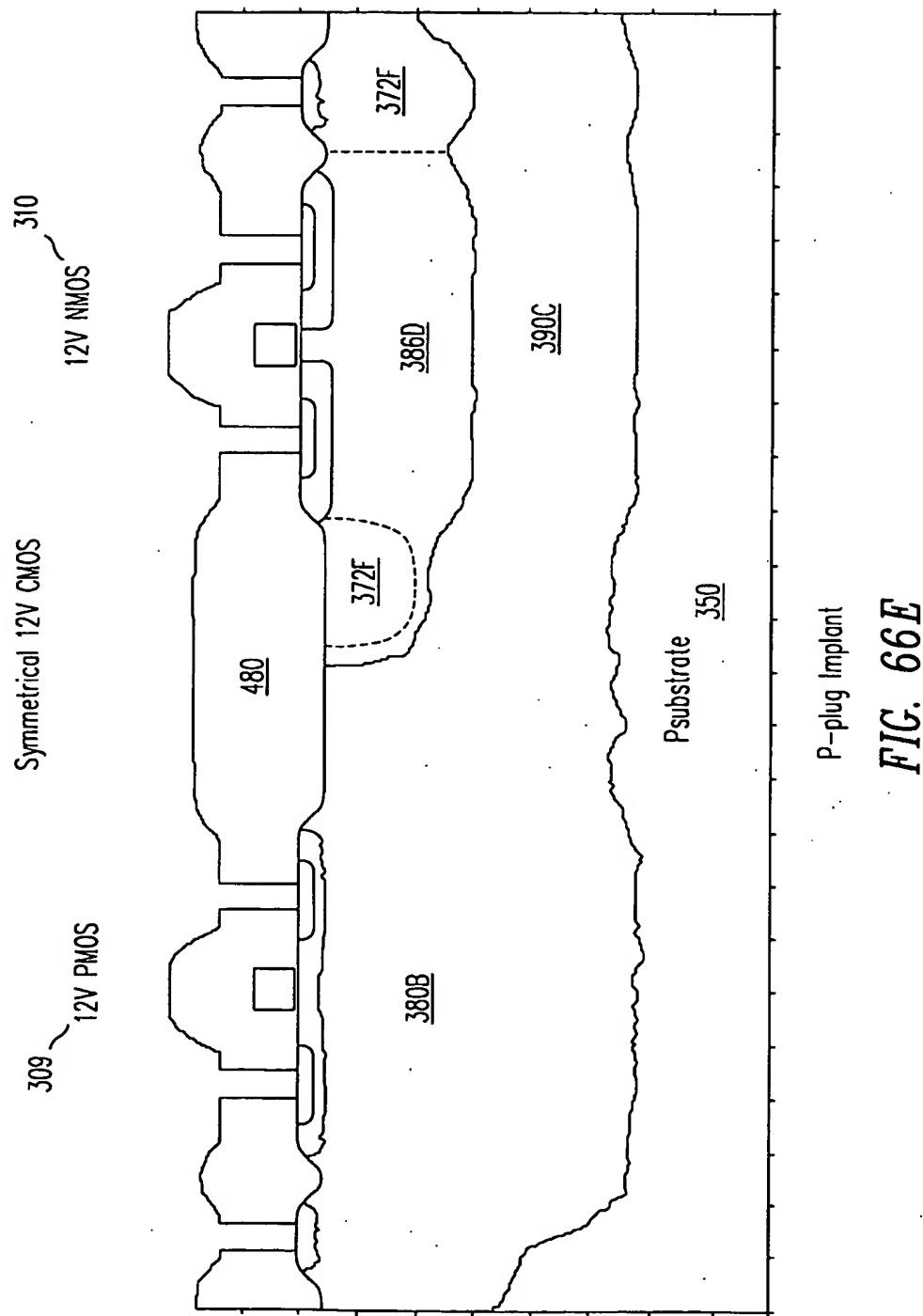


FIG. 66E

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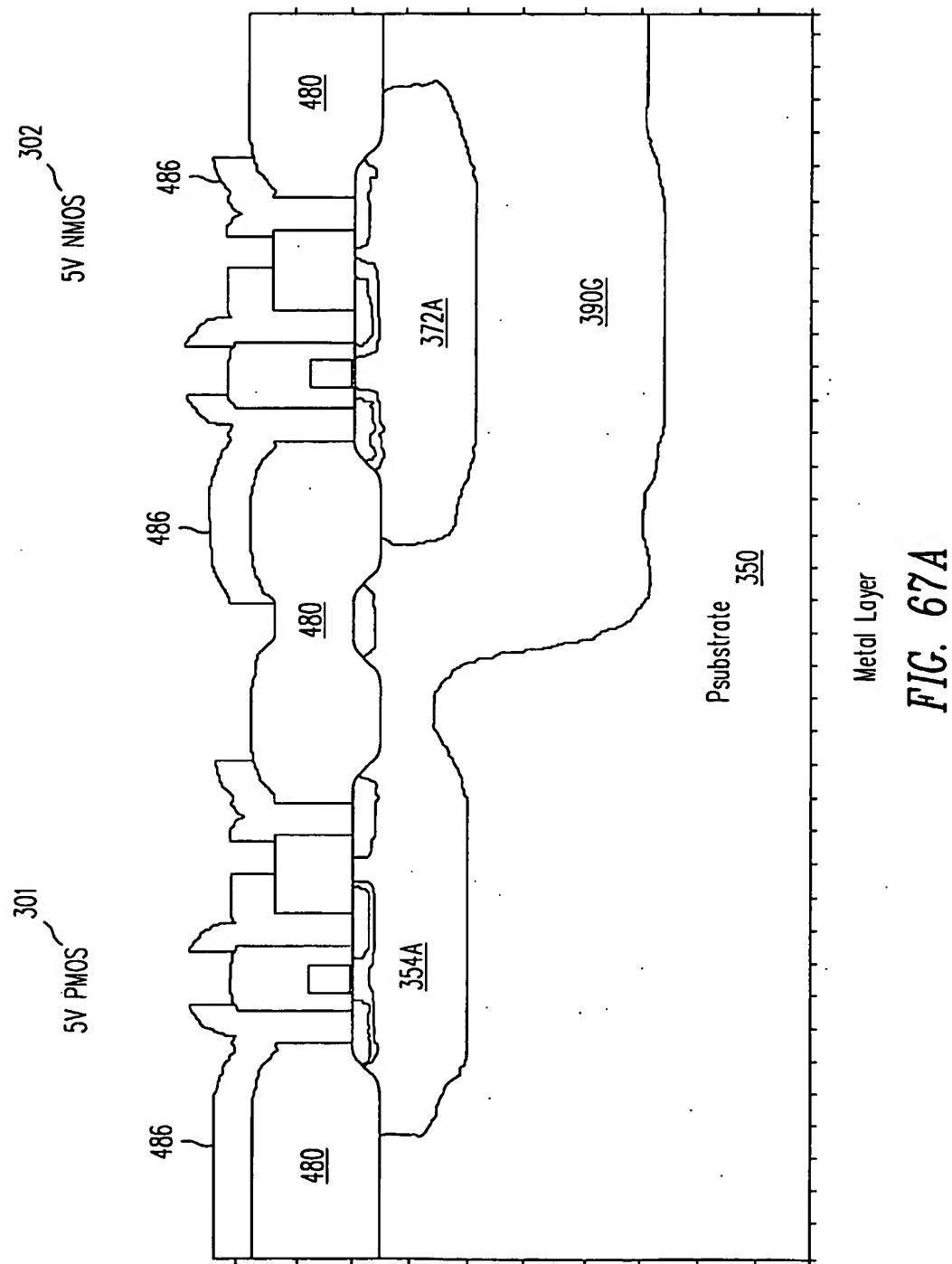
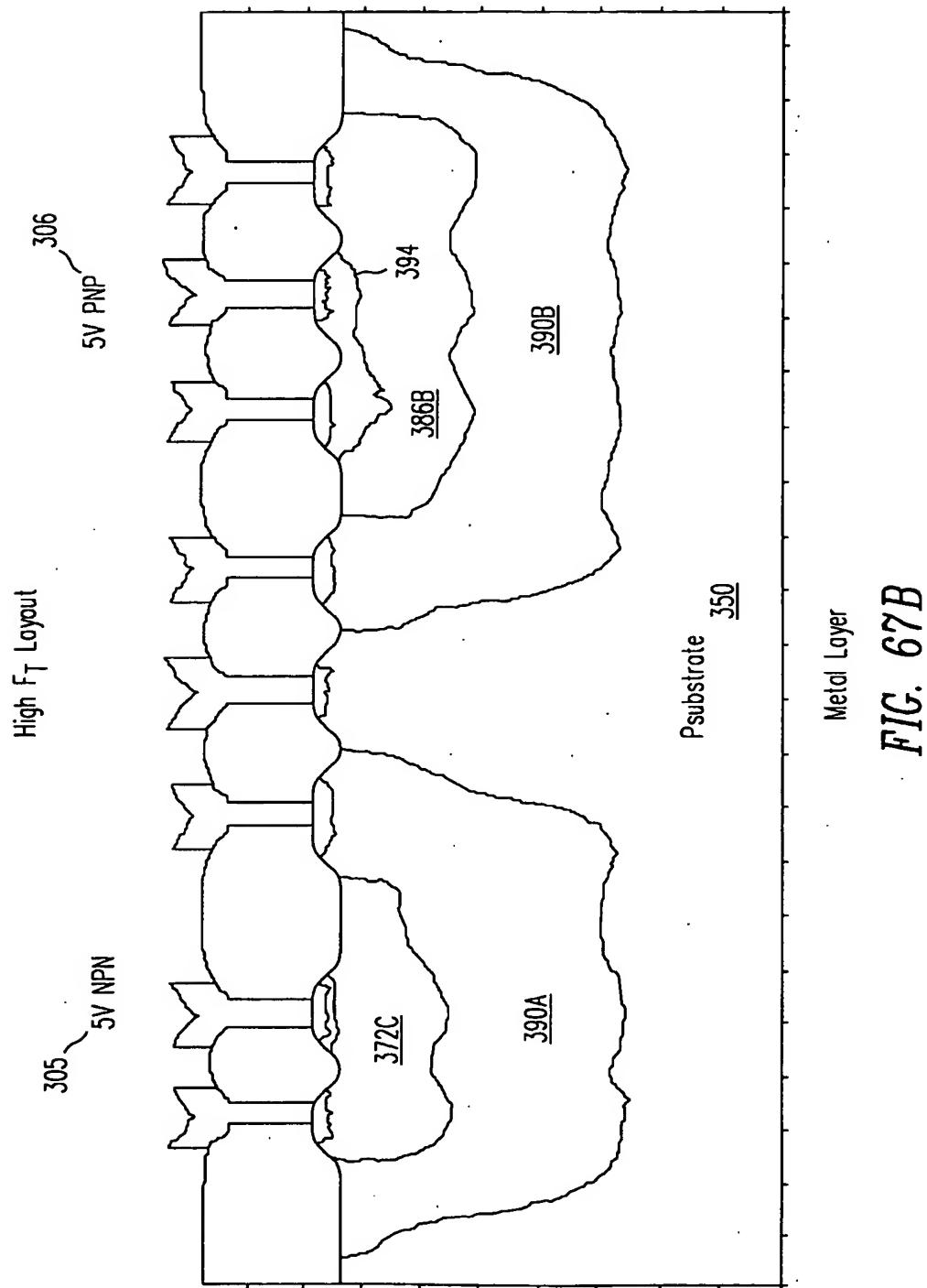
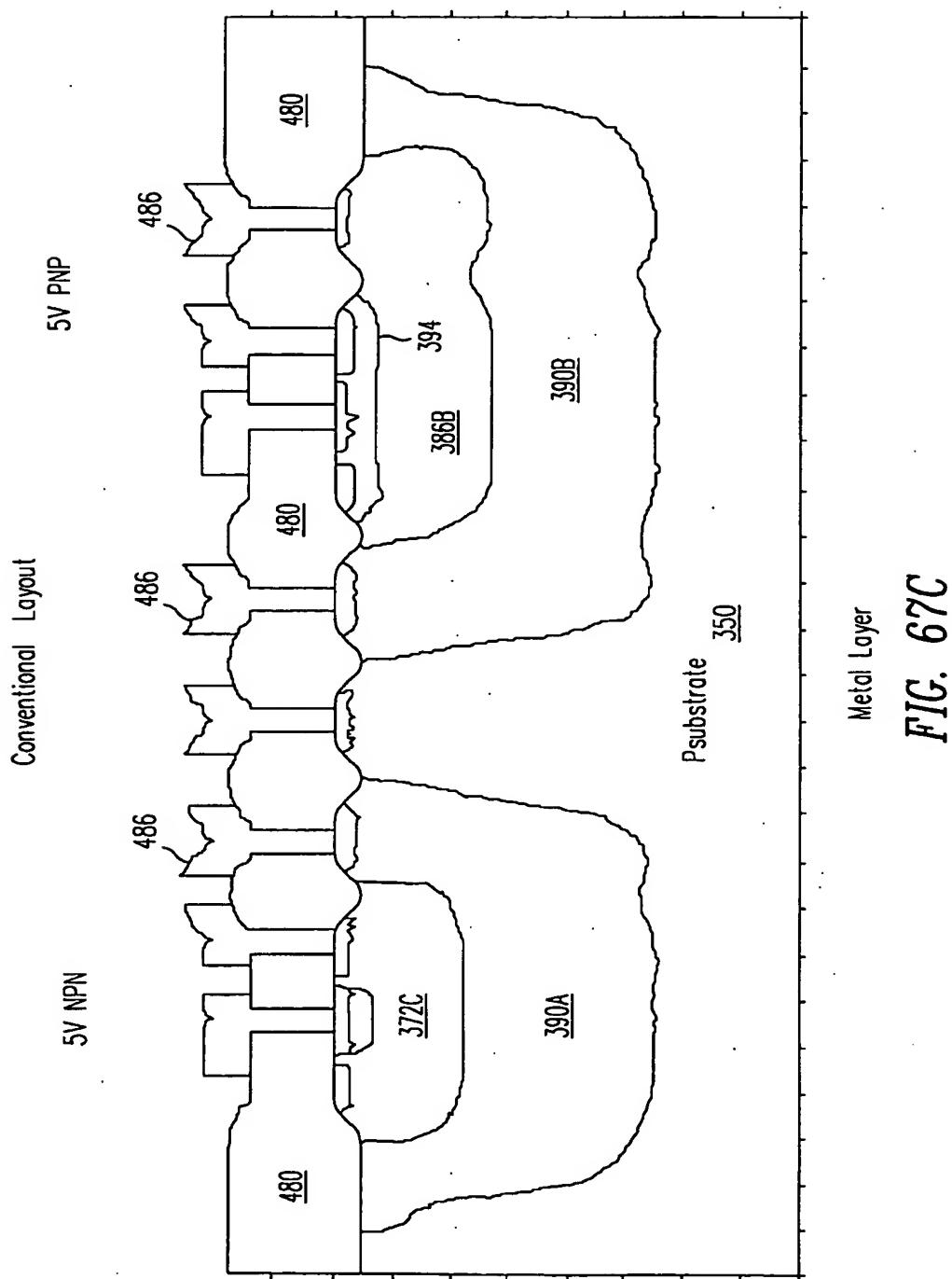
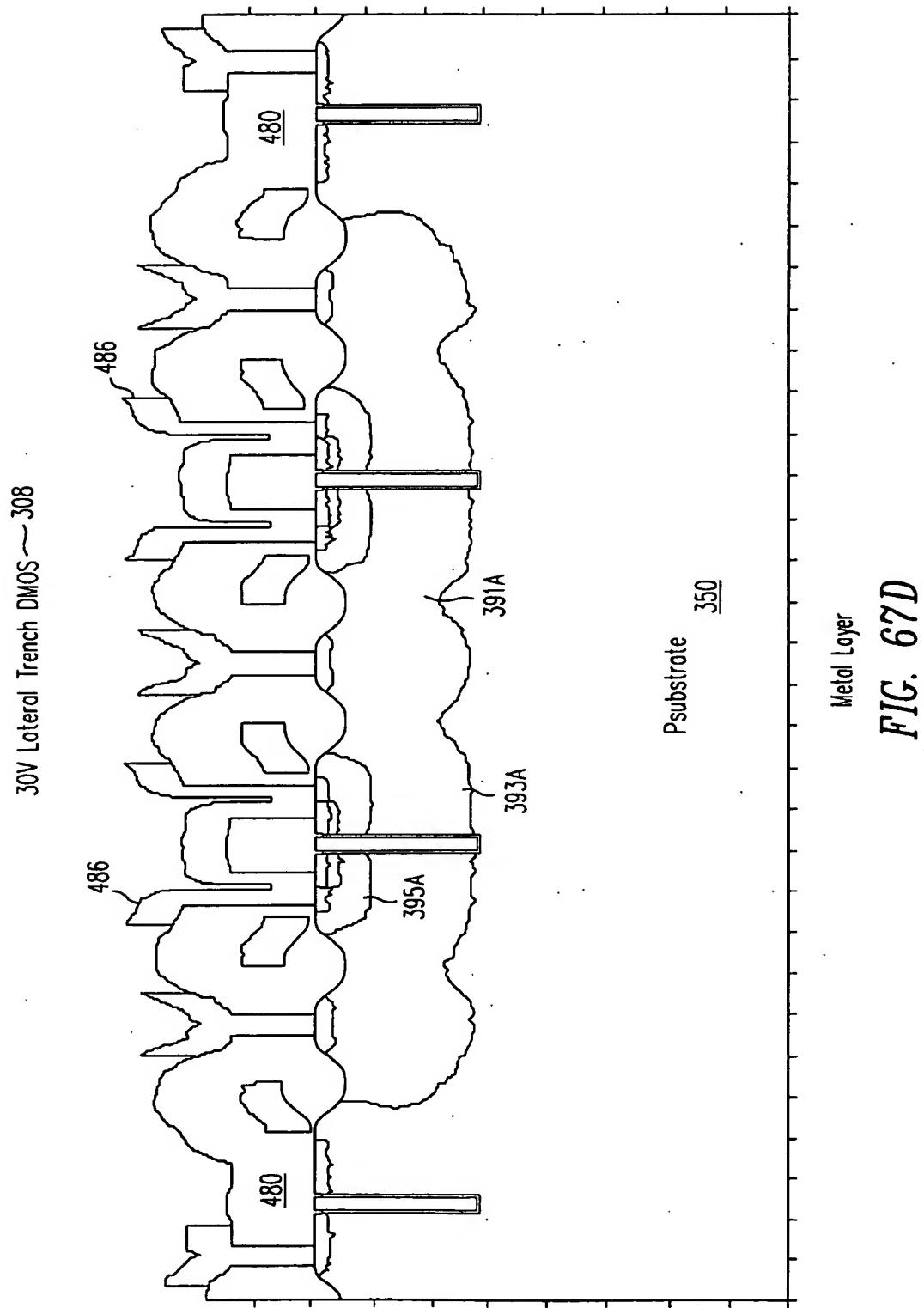


FIG. 67A





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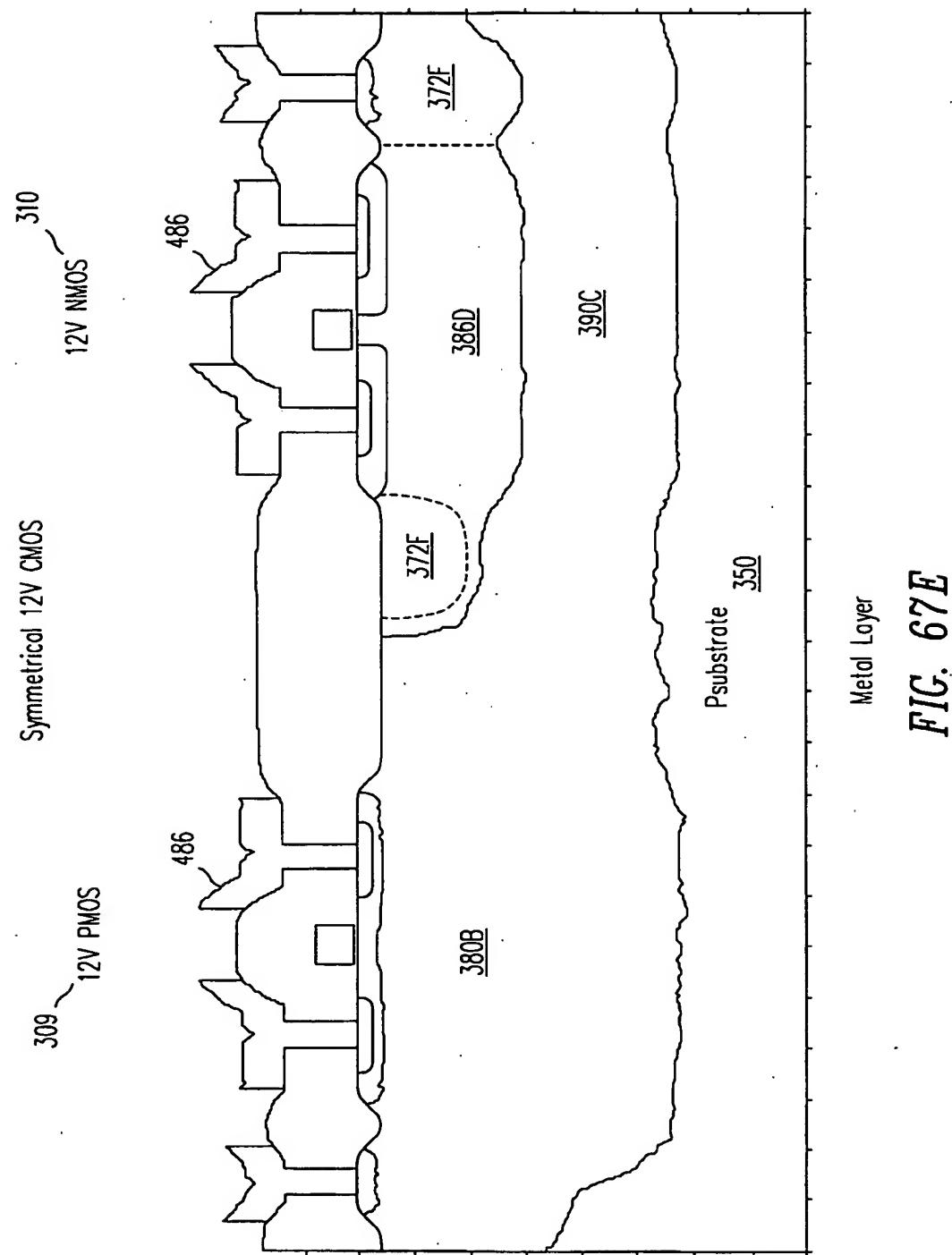


FIG. 67E